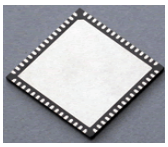
SPD1078

**32-bit MCU with 12-bit ADC, 3 PGAs,
Single supply up to 60V with fully integrated power management
and 3-phase Pre-Driver**

Revision 9 – May 2021

Features



QFN64 (8 x 8 mm)

- 32-bit CPU Core
  - 150MHz maximum frequency
- Memories
  - 512KB in-package flash
  - 512 Bytes OTP flash
  - 48KB on-chip SRAM
- Pre-Driver Module
  - 3 Phase Pre-Driver for BLDC motor application with 60V max Vin
  - Integrated power diode
  - Integrated charge pump to support 100% duty cycle
  - Max 2A Driving capability on each phase
  - Programmable output swing 8 to 18V
  - 6 VDS monitor to have current limit on each of the external FET
- Power management module
  - 60V input, 3.3V output, 600mA synchronous buck DCDC, efficiency up to 85%
  - Integrated Power FETs and bootstrap diode
  - PFM mode at light load with optional forced PWM mode
  - 60V input, 9V, 10V, 12V, 15V, 18V output programmable, 50mA LDO
  - Brown-out-detector on each of the supply voltage
- Clock, reset and supply management
  - Single power supply
  - Power-On Reset (POR)
  - 4 to 16 MHz external crystal oscillator
  - Two 24 MHz internal factory-trimmed RC oscillators
  - PLL for CPU clock
- 12-bit A/D converters (up to 7 channels)
  - As low as 125 ns conversion time
  - Conversion range: 0 to 3.65 V
  - Differential sample
  - Dual-sample and hold capability
  - Open/short detection for safety
  - Temperature sensor
- Programmable gain amplifier (PGA)
  - Three integrated internal PGAs
  - Programmable Gains
    - Single-ended: 2, 4, 8, 16
    - Differential: 4, 8, 16, 32
  - Typical 600 ns settling time
- Analog comparator
  - Six high-speed comparators
  - Output with digital deglitch filter
  - Two DACs as reference
  - Out of range voltage protection
- PWM
  - Seven enhanced PWM modules
  - 14 PWM outputs total
  - Flexible waveform generation with phase lead/lag control
  - All events can trigger ADC conversion
- Up to 23 GPIO Pins
  - Configurable pull-up/pull-down resistors
  - Programmable digital input deglitch filter

- Enhanced Capture Module (ECAP)
  - Flexible input capture pin
  - Four 32-bit capture registers
  - Capture and PWM mode selection
- Debug mode
  - Serial wire debug (SWD) & JTAG interfaces
- 6 Timers
  - Three 32-bit general-purpose timers
  - Two 32-bit watchdog timers
  - SysTick timer 24-bit down-counter
- Communication interfaces
  - UART x 1 , SPI x 1, I^2C x 1
- Security Modules
  - CRC x 1, AES x 1
- Operating temperature
  - Junction temperature: -40 to +125 ^oC
  - Operating temperature: Industrial Class

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1 Device overview

SPD1078 is a SiP (System in a Package) device integrating MCU, Pre-Driver module and power management module to have "all-in-one" chip for BLDC motor driving application.

The MCU incorporates a 32-bit high-performance processor with a software-programmable clock rate as high as 150 MHz, 48 KB CODE/SRAM, in-package flash with 512 KB, and an extensive range of enhanced I/Os and peripherals. The device offers a 12-bit ADC, three PGAs, seven enhanced PWMs, three general purpose 32-bit timers, as well as standard and advanced communication interface: an UART, an I2C and a SPI. These features make the SPD1078 ideal for applications such as inverter.

The Pre-Driver module provides three half-bridge pre-drivers, with programmable charging/discharging current capability up to 2A. Integrated Charge Pump will help to support 100% Duty Cycle.

The Power management module includes a 60V Max input, 3.3V 600mA output synchronous buck, 50mA LDO with output from 9 ~ 18V programmable and Brown-out-Detection for each of the power level.

In SPD1078, the internal MCU controls the GATE Driver. The connection between the MCU and the Driver is shown in Figure 2.

Figure 1. SPD1078 block diagram

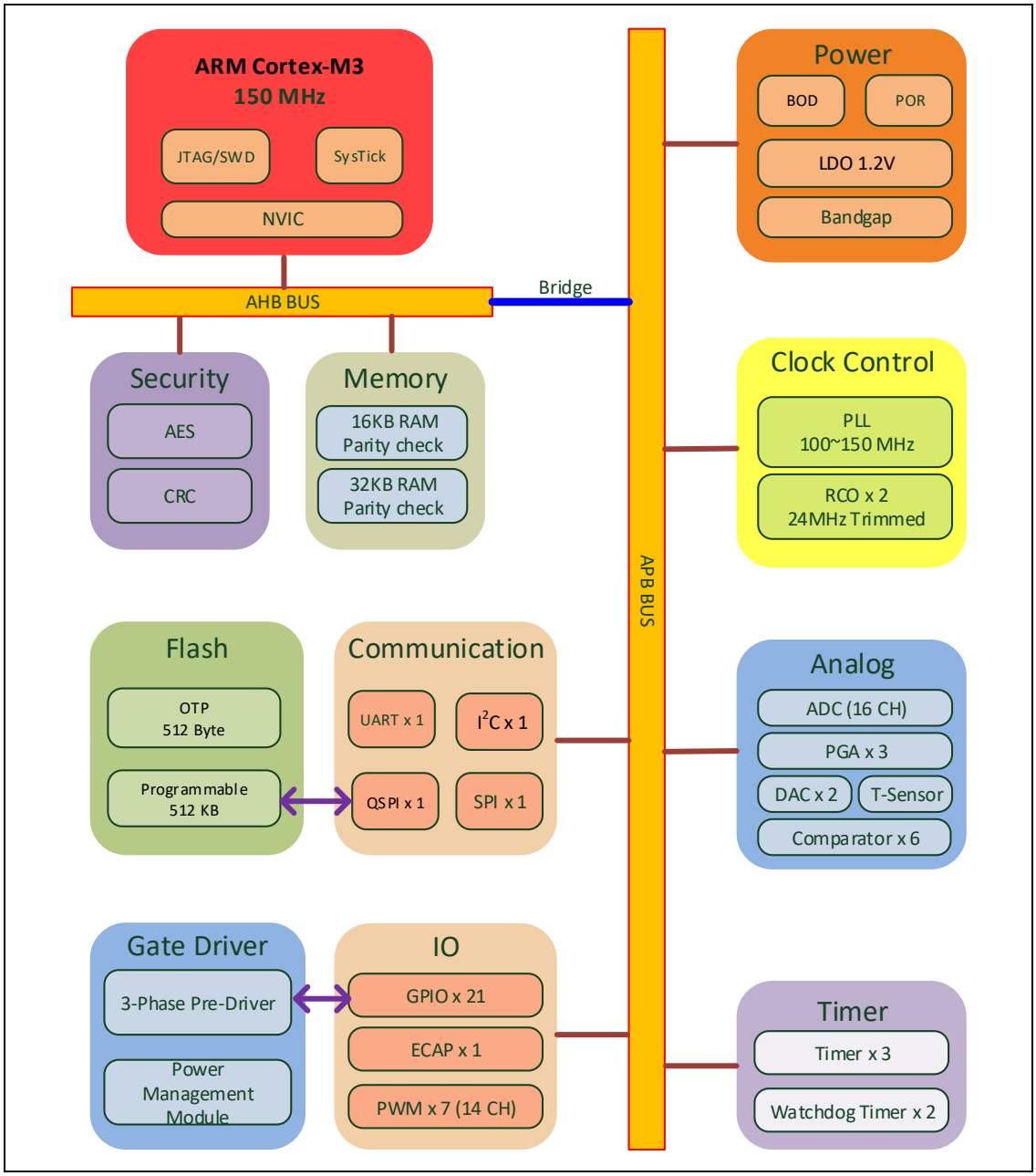


Figure 2. MCU and Pre-Driver connection diagram

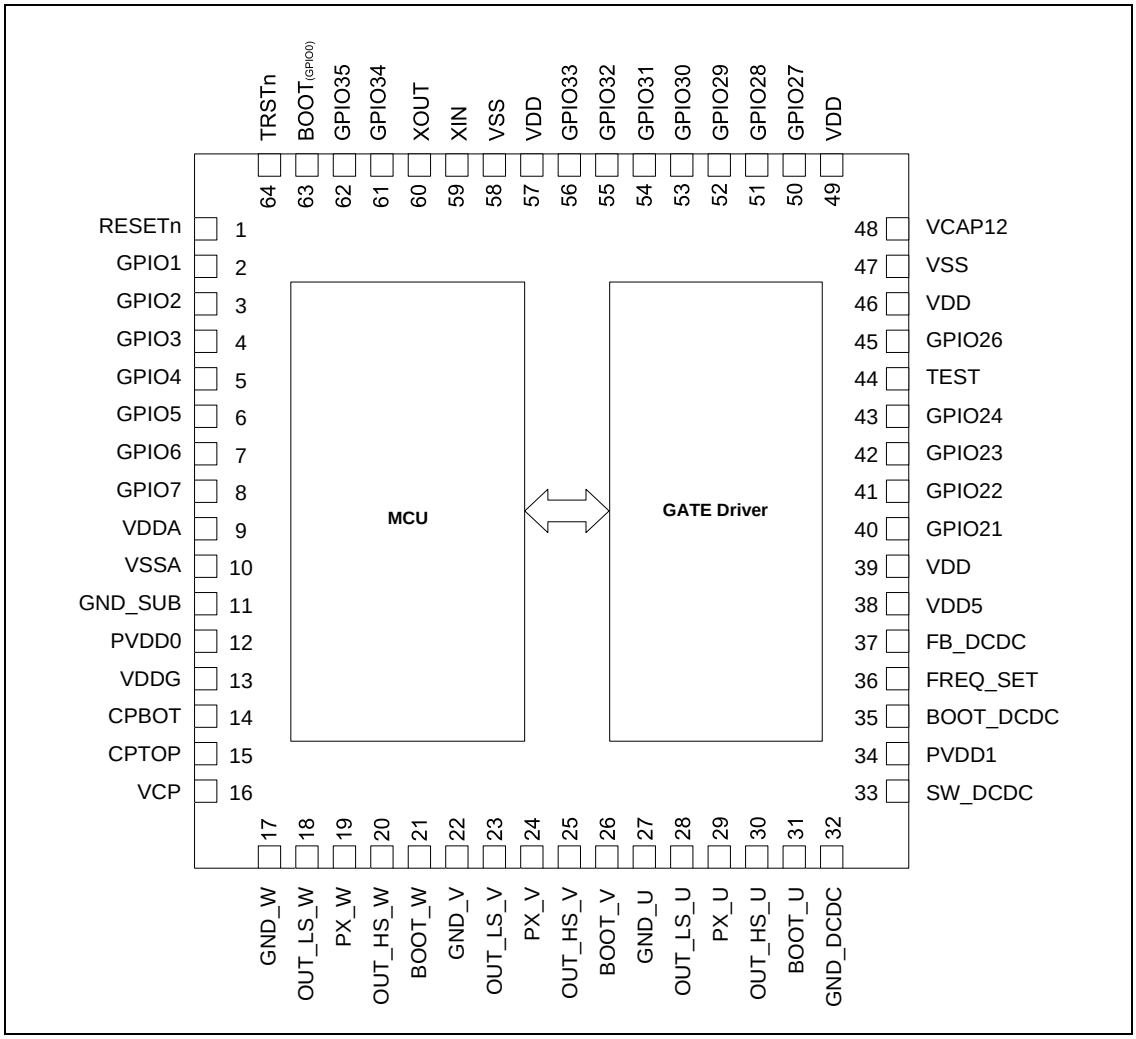
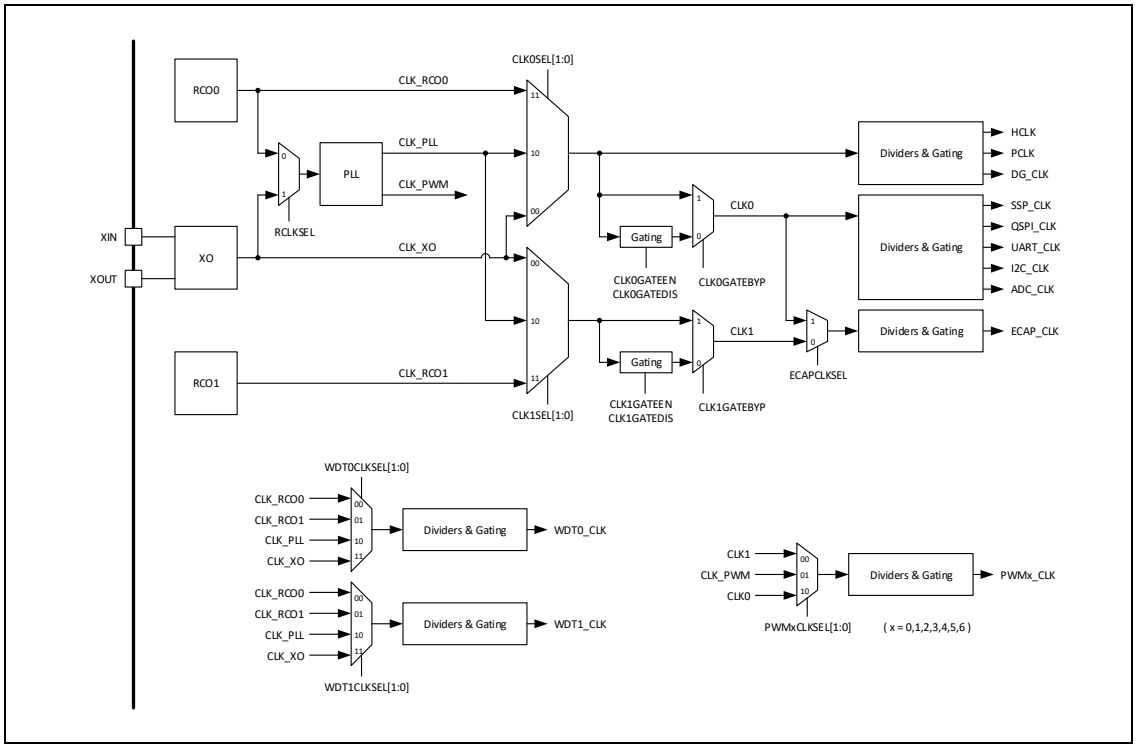
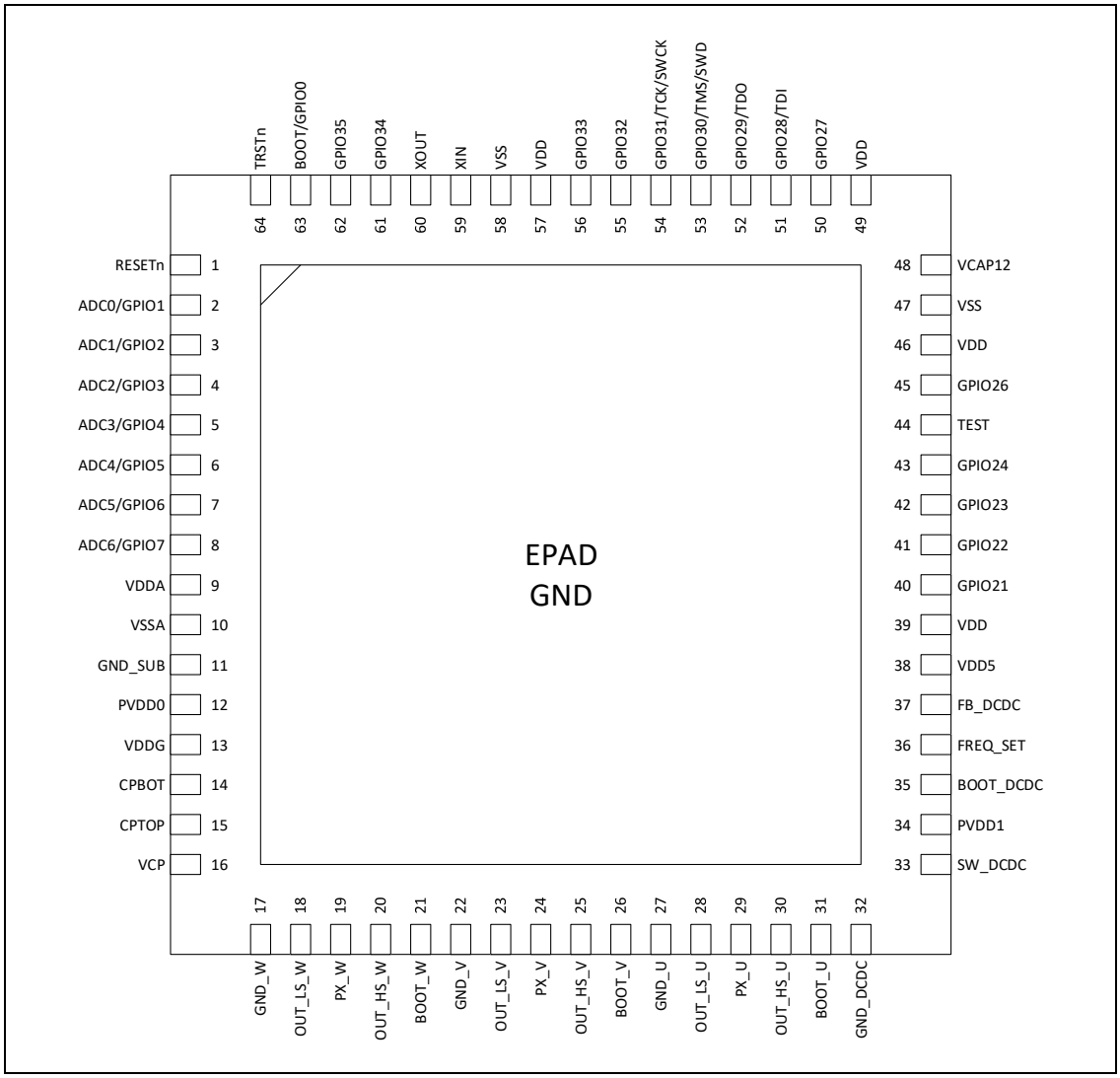


Figure 3. Clock tree



2 Pin-outs and pin description

Figure 4. SPD1078 QFN64L pin-out



(1) **Note: when TRSTn is HIGH, GPIO28 ~ GPIO31 pins work as Debug interface and can't be configured as other functions.**

Table 1. SPD1078 pin definitions

Pin	Signal	Type(1)	Description
1	RESETn	I	Device reset pin, reset the device when low
2	ADC0	AI	ADC channel 0 input
	GPIO1	I/O	General-purpose input/output 1
	PWMSYNCI	I	PWM synchronization pulse input
	PWMSYNCO	O	PWM synchronization pulse output
	I2C_SDA	I/O	I2C data
3	ADC1	AI	ADC channel 1 input
	GPIO2	I/O	General-purpose input/output 2
	PWM5B	O	PWM5 output B

Table 1. SPD1078 pin definitions (continued)

Pin	Signal	Type[1]	Description
4	ADC2	AI	ADC channel 2 input
	GPIO3	I/O	General-purpose input/output 3
	PWM5A	O	PWM5 output A
5	ADC3	AI	ADC channel 3 input
	GPIO4	I/O	General-purpose input/output 4
	PWM6B	O	PWM6 output B
6	ADC4	AI	ADC channel 4 input
	GPIO5	I/O	General-purpose input/output 5
	PWM6A	O	PWM6 output A
7	ADC5	AI	ADC channel 5 input
	GPIO6	I/O	General-purpose input/output 6
	PWM4B	O	PWM4 output B
8	ADC6	AI	ADC channel 6 input
	GPIO7	I/O	General-purpose input/output 7
	PWM4A	O	PWM4 output A
9	VDDA	S	Analog power pin
10	VSSA	S	Analog ground pin
11	VSS	S	Main Ground
12	PVDD0	S	Main Supply Voltage，up to 60V
13	VDDG	S	VDDG LDO Output, 8V ~ 18V Programmable, 2.2uF Cap recommended
14	CPBOT	S	Charge Pump Flying Capacitor Bottom Plate Voltage
15	CPTOP	S	Charge Pump Flying Capacitor Top Plate Voltage
16	VCP	S	Charge Pump Output, 2.2uF cap recommended **The maximum output voltage is PVDD0 + VDDG**
17	GND_W	O	Driver GND, External Low side FET Source
18	OUT_LS_W	O	Low Side FET Gate Drive
19	PX_W	O	Power FET Switching Node
20	OUT_HS_W	O	High Side FET Gate Drive
21	BOOT_W	O	Bootstrap Pin
22	GND_V	O	Driver GND, External Low side FET Source
23	OUT_LS_V	O	Low Side FET Gate Drive
24	PX_V	O	Power FET Switching Node
25	OUT_HS_V	O	High Side FET Gate Drive
26	BOOT_V	O	Bootstrap Pin
27	GND_U	O	Driver GND, External Low side FET Source
28	OUT_LS_U	O	Low Side FET Gate Drive
29	PX_U	O	Power FET Switching Node
30	OUT_HS_U	O	High Side FET Gate Drive
31	BOOT_U	O	Bootstrap Pin

Table 1. SPD1078 pin definitions (continued)

Pin	Signal	Type[1]	Description
32	GND_DCDC	S	DCDC Ground
33	SW_DCDC	S	DCDC Switching Node
34	PVDD1	S	DCDC power train supply
35	BOOT_DCDC	S	Bootstrap Pin for DCDC
36	FREQ_SET	S	Frequency Set Pin, 100Kohm resistor for 450kHz
37	FB_DCDC	S	DCDC feedback node
38	VDD5	S	5V LDO output, 2.2uF cap recommended
39	VDD	S	Digital power
40	GPIO21	I/O	General-purpose input/output 21
	SPIMI	I	SPI master in
	SPISO	O	SPI slave output
	PWM4B	O	PWM4 output B
41	GPIO22	I/O	General-purpose input/output 22
	SPIMO	O	SPI master out
	SPISI	I	SPI slave in
	PWM4A	O	PWM4 output A
42	GPIO23	I/O	General-purpose input/output 23
	PWM0B	O	PWM0 output B
	COMP0LOUT	O	Output of comparator 0 of low-voltage
43	GPIO24	I/O	General-purpose input/output 24
	PWM0A	O	PWM0 output A
44	TEST	-	Test pin. Reserved for Spintrol.
45	GPIO26	I/O	General-purpose input/output 26
	I2C_SDA	I/O	I2C data
	PWMSYNCI	I	PWM synchronization pulse input
	ADCSOCAO	O	ADC start-of-conversion A
46	VDD	S	Digital power
47	VSS	S	Digital ground
48	VCAP12	S	1.2 V power
49	VDD	S	Digital power
50	GPIO27	I/O	General-purpose input/output 27
	I2C_SCL	I/O	I2C clock
	PWMSYNCO	O	PWM synchronization pulse output
	ADCSOCBO	O	ADC start-of-conversion B
51	GPIO28	I/O	General-purpose input/output 28
	PWM1A	O	PWM1 output A
	TDI	I	JTAG data input **When TRSTn is HIGH, this pin always works as TDI**

Table 1. SPD1078 pin definitions (continued)

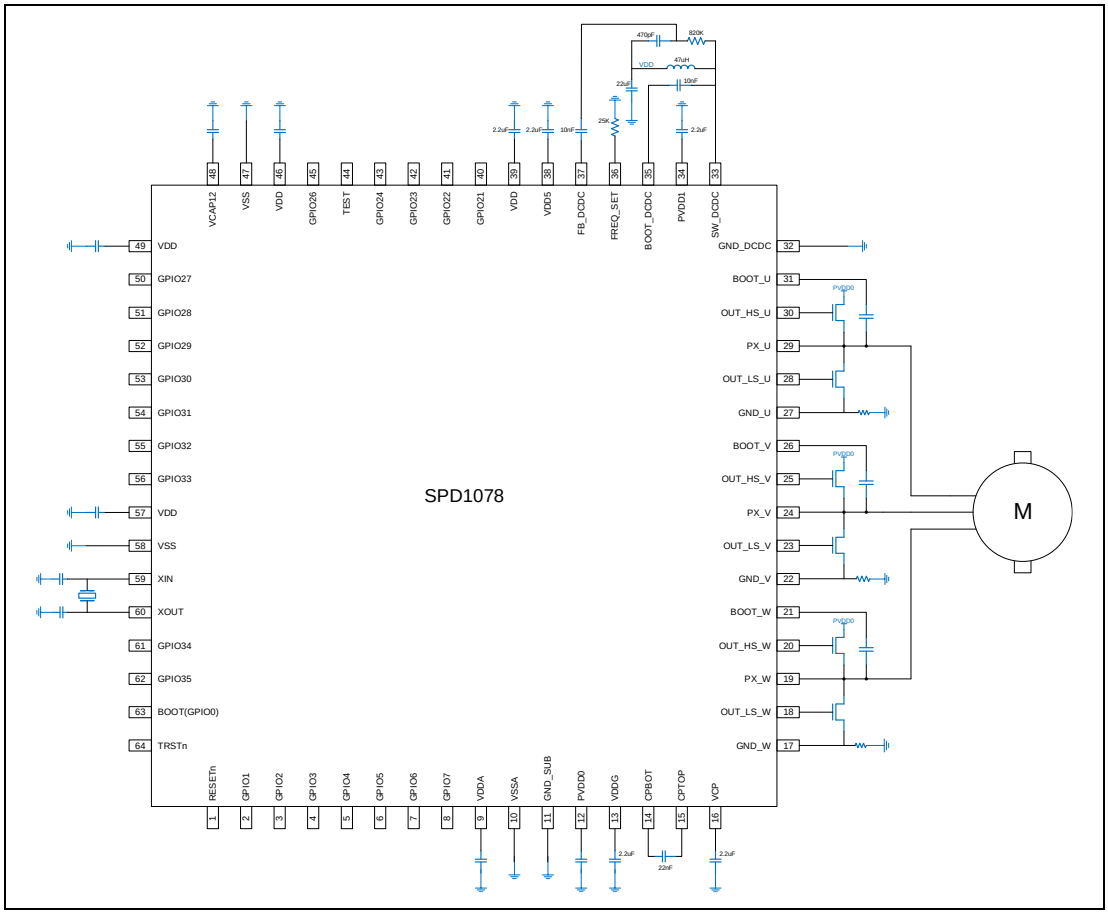
Pin	Signal	Type[1]	Description
52	GPIO29	I/O	General-purpose input/output 29
	PWM1B	O	PWM1 output B
	COMP0HOUT	O	Output of comparator 0 of high-voltage
	TDO	O	JTAG data output **When TRSTn is HIGH, this pin always works as TDO**
53	GPIO30	I/O	General-purpose input/output 30
	PWM2A	O	PWM2 output A
	TMS/SWD	I/O	JTAG mode select or SWD data **When TRSTn is HIGH, this pin always works as TMS/SWD**
54	GPIO31	I/O	General-purpose input/output 31
	PWM2B	O	PWM2 output B
	TCK/SWCK	I	JTAG clock or SWD clock **When TRSTn is HIGH, this pin always works as TCK/SWCK**
55	GPIO32	I/O	General-purpose input/output 32
	PWM3A	O	PWM3 output A
	PWMSYNCI	I	PWM synchronization pulse input
	PWMSYNCO	O	PWM synchronization pulse output
	SPICLK	I/O	SPI clock input/output
56	GPIO33	I/O	General-purpose input/output 33
	PWM3B	O	PWM3 output B
	UART_RXD	I	UART receive data
	SPI_FRM	I/O	SPI frame signal
57	VDD	S	Digital power
58	VSS	S	Digital ground
59	XIN	AI	External oscillator input
60	XOUT	AO	External oscillator output
61	GPIO34	I/O	General-purpose input/output 34
	UART_TXD	O	UART transmit data
	UART_RXD	I	UART receive data
62	GPIO35	I/O	General-purpose input/output 35
	UART_RXD	I	UART receive data
	I2C_SDA	I/O	I2C data
	UART_TXD	O	UART transmit data
63	BOOT(GPIO0)	I/O	Boot pin (General-purpose input/output 0)
	UART_TXD	O	UART transmit data
	I2C_SCL	I/O	I2C clock
64	TRSTn	I	JTAG reset pin, reset the JTAG when low

(1) I = digital input, O = digital output, AI = analog input, AO = analog out, S = supply.

(2) All GPIO pins can be configured as ECAP input.

(3) All GPIO pins can be configured as ECAP output.

Figure 5. SPD1078 typical application diagram



3 Feature descriptions

3.1 Micro control unit (MCU)

The processor has been developed to provide a platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The SPD1078 integrates a processor core that runs up to 150 MHz.

3.2 Embedded SRAM

The SPD1078 has implemented 48 KB of CODE/DATA SRAM memory. The SRAM can be accessed (read/write) at CPU clock speed with 0 wait states.

3.3 In-package Flash

The SPD1078 is integrated with 512 KB in-package serial flash memory for storing programs and data, which is connected to QSPI interface. The features of the serial flash include:

- Total 512 KB flash memory
- 200 Mbps maximum serial data rate in Quad mode with 50 MHz operating clock
- Write protect all or portions of flash memory
- Sector erase (4KB) and Block erase (32 or 64 KB)
- Page program up to 256 bytes

3.4 Nested vectored interrupt controller (NVIC)

The SPD1078 embeds a nested vectored interrupt controller able to handle up to 46 maskable interrupt channels (not including the 16 interrupt lines of Cortex-M3) and 16 programmable priority levels.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Processing of *late arriving* higher priority interrupts
- Support for tail-chaining
- Interrupt entry restored on interrupt exit with no instruction overhead

3.5 External interrupt/event controller

The SPD1078 provides a flexible external pin interrupt or event trigger mechanism. Any GPIO pin can be programmed as an external interrupt or event trigger source. In addition, any GPIO interrupt can be configured as edge-triggered or level-triggered.

3.6 Power supply and Reset

The SPD1078 supports single power supply up to 60V, which powers the IOs, internal voltage regulators and analog circuitry on chip. There are no special power-up sequencing requirements for the SPD1078.

The SPD1078 has a global reset pin as well as an integrated power-on reset (POR) circuitry. The POR circuitry guarantees all power-up reset sequence requirements and makes the device easy to use.

3.7 Brown-out detect

The device features an embedded brown-out detector (BOD) that monitors the V_{DD} power supply and compare it to the programmable pre-set value. An interrupt or reset can be generate when V_{DD} is higher or drops below the pre-set value. The interrupt service routine then generate a warning message and/or put the MCU into a safe state. The BOD is enabled by software.

3.8 Clocks

System clock selection is performed on startup, however the internal 24 MHz RC oscillator is selected as default CPU clock on reset. An external 4 - 16 MHz oscillator can be selected.

The device implements a fractional phase-lock loop (PLL) for high frequency clock generation. The PLL can take the internal RC oscillator or external clock as the input reference clock. The PLL can provide 100 - 150 MHz clock for the core and PWM modules.

Several pre-scalers allow the configuration of the AHB, APB and the peripherals frequency. The maximum allowed frequency of the APB is 37.5 MHz. The peripherals frequency should not lower than APB bus frequency. See Figure 3 for details on the clock tree.

3.9 Boot mode

The boot code is located in on-chip ROM memory. After a reset, the microprocessor begins code execution from this ROM. The boot pin is used to select one of the two boot options:

- Boot from in-package Flash (boot pin = 1): the boot loader copies user codes in the in-package flash to embedded SRAM, then runs code from SRAM
- ISP mode (boot pin = 0): the boot loader reprograms the in-package flash by using UART

Note: The boot pin can be configured as GPIO0.Be careful to use it in applications and can only be configured as output. Please make sure the pin level is high while the device is resetting or the device will enter ISP mode.

3.10 General-purpose IOs (GPIOs)

The SPD1078 can be configured to support as many as 23 multi-purpose GPIO pins. Each GPIO pin can be configured by software as input, as output or as peripheral alternate function. It features:

- Each GPIO pin has configurable internal pull-up and pull-down resistors

- Each GPIO pin has a programmable digital input deglitch filter

Note 1: Boot pin can be configured as GPIO0.
Note 2: GPIO25 is test pin reserved for Spintrol.

3.11 Timers and watchdogs

The SPD1078 device includes three general-purpose timers, two watchdog timers and a SysTick timer.

General-purpose timers

The SPD1078 includes three identical 32-bit general-purpose timers. Each general-purpose timer consists of a 32-bit auto-reload down-counter. An interrupt would be generated when the counter reaches zero if it is enabled. The clock of general-purpose timer is from APB clock (PCLK). However, each general-purpose timer can also capture external input as timer clock or enable signal.

Watchdogs

The SPD1078 implements two watchdogs. Each watchdog is based on a 32-bit down-counter. Each watchdog can be clocked from internal RC oscillator, external oscillator or PLL clock. Each watchdog can generate a reset or an interrupt when the counter reaches the given time-out value. Each watchdog counter can be frozen or free-running in debug mode.

SysTick Timer

This timer is dedicated for OS, but could also be used as a standard down-counter. It features:

- A 24-bit down-counter
- Auto-reload capability
- Mask-able system interrupt generation when the counter reaches 0

3.12 UART

The SPD1078 has an UART module that is functionally compatible with the 16550A and 16750 industry standards. It features:

- Ability to add or delete standard asynchronous communication bits (start, stop and parity) in the serial data
- 7- or 8- bit characters
- Even, odd or no parity detection
- 1 stop-bit generation
- Baud-rate generation up to 3.6 Mbps
- 64-byte transmit FIFO
- 64-byte receive FIFO
- Auto baud-rate detection

3.13 I^2C

The I^2C bus interface complies with the common I^2C protocol and can operate in standard mode (with data rates up to 100 Kb/s) and fast mode (with data rates up to 400 Kb/s). It features:

- Three speeds: Standard mode (100 Kb/s), Fast mode (400 Kb/s) and High-Speed mode (2 Mb/s)
- Clock synchronization
- Master or slave I^2C operation
- 7- or 10-bit addressing
- 7- or 10-bit combined format transfers
- 16 x 32-bit deep transmit and receive buffers, respectively

3.14 SPI

The SPI allows half/full-duplex, synchronous, serial communication with external devices. It features:

- Full-duplex synchronous transfers
- Master or slave operation
- 1 to 32-bit transfer frame format selection
- 25 Mbps maximum communication speed
- MSB-first data order
- Programmable clock polarity and phase
- Transmit and receive FIFOs

3.15 ADC

One 12-bit analog-to-digital convert is embedded into SPD1078 and has up to 8 external channels. The temperature sensor, internal powers and PGA outputs can be selected as ADC input channels. These inputs are multiplexed. The ADC core has two independent built-in sample-and-hold (S/H). Each S/H has two input channels, which is suitable for differential sampling.

The events generated by the general-purpose timers and the PWM outputs can be internally connected to the ADC start trigger. A brief bullet summary of ADC properties follows.

- 12-bit resolution
- 125 ns minimum conversion time and independent configurable sampling time
- Differential sampling
- Dual-sample and hold capability
- Simultaneous sampling and sequential sampling modes supported
- Full range analog input: 0 V to 3.65 V
- Reference voltage can be selected from internal or external
- Input short and disconnection detection for safety

3.16 Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The temperature sensor is internally connected to the ADC input channel which is used to convert the sensor output voltage into a digital value.

3.17 PGAs

Three flexible programmable gain amplifiers (PGAs) are embedded into SPD1078 and shares up to 16

channels. The temperature sensor and internal 1.2V power can be selected as PGA input channels. These inputs are multiplexed. Each PGA outputs are connected to ADC input channel.

- Programmable gains: Differential mode - 4, 8, 16, 32; Single-ended mode - 2, 4, 8, 16
- Settling time: 400 ns to 800 ns

3.18 Analog comparators

The SPD1078 has three pairs high-speed windowed comparators. Each comparator uses the internal DAC as reference for monitoring PGA inputs or outputs. Two comparators are designed for each PGA: one is monitoring too-high voltage, the other is monitoring too-low voltage. The comparator output is routed to the PWM Trip Zone modules.

- 50 ns typical response
- Programmable hysteresis
- Output with digital deglitch filter

3.19 PWMs

The SPD1078 integrates seven PWM modules and supports 14 PWM channels. Three PWM modules are assigned to drive internal pre-drivers much involvement of processor core, the PWMs can generate complex pulse width waveforms.

Each PWM module supports the following features:

- Dedicated 16-bit time-base counter with period and frequency control
- Each PWM module can generate two outputs with single-edge operation, dual-edge symmetric operation or dual-edge asymmetric operation
- All events can trigger both CPU interrupts and ADC start of conversion
- Programmable phase-control support for lag or lead operation relative to other PWM modules
- Dead-band generation with independent rising and falling edge delay control
- Programmable trip zone allocation of both cycle-by-cycle trip and one-shot trip on fault conditions
- A trip condition can force either high, low, or high-impedance state logic levels at PWM outputs
- Comparator module outputs and trip zone inputs can generate events, filtered events, or trip conditions

3.20 ECAP

The enhanced capture (ECAP) module is essential in systems where accurate timing of external events is important. The SPD1078 has implemented an ECAP module with following features:

- Flexible input capture pin: each GPIO can be configured as capture pin
- 32-bit time base counter
- 4 x 32-bit time-stamp capture registers
- 4-stage sequencer that is synchronized to external events
- Independent edge polarity (rising/falling edge) selection for all 4 events
- Interrupt capabilities on any of the 4 capture events

3.21 Cyclic redundancy check (CRC)

The SPD1078 has a hardware CRC calculation unit. The CRC module is used to verify data transmission or storage integrity. It features:

- 32-bit parallel bit stream input, and up to 32-bit CRC output
- Supports up to 2^{32} byte length for CRC calculation
- Four CRC standard polynomials supported

3.22 Advanced encryption standard (AES) engine

The AES engine provides fast hardware encryption and decryption services. The main features are as follows:

- Supports as many as six block cipher modes: ECB, CBC, CTR, CCM*, MMO, and Bypass
- Supports 128-, 192-, and 256-bits key size
- Error indication for each block cipher mode
- Separate 4 x 32-bit input and output FIFOs

3.23 Serial wire JTAG debug port (SWJ-DP)

The MCU SWJ-DP interface is embedded and is a combined JTAG and serial wire debug port. The SWJ-DP interface enables either a serial wire debug or a JTAG probe to be connected to the target. The debug port can be disabled when enabling SPD1078 certain security feature.

3.24 Pre-Driver module

Pre-driver will “amplify” PWM with up to 2A driving capability, output voltage swing is 0~VDDG (VDDG provided by on-chip VDDG LDO with configurable 9V,10V,12V,15V,18V output level). Max driving current can be halved by setting registers for efficiency. The pre-driver uses bootstrap architecture with integrated power diode. A charge pump keeps replenishing charge on the bootstrap capacitor when external high side FET is on to support 100% duty cycle. Six PWM signals (high side and low side of 3 phases) can be controlled by MCU independently, while the internal handshake circuits will make sure high side and low side will not turn on at the same time for safety. Six Vds-monitors will assert over current on each of the external power FET if the drain-to-source voltage is higher than threshold which can be programmed.

3.25 Power management module

SPD1078 integrates power management module including one Buck DCDC (3.3V, 600mA), 12V LDO (40mA), brown-out-detection at all power levels, allowing for single DC power input application.

A fully integrated buck DCDC converter provides 3.3V supply to MCU, with no external power FET or diode. It can also provide 3.3V supply to other circuits on the board, as long as total current out of 3.3V supply does not exceed 600mA. If there is already 3.3V supply from the board, the buck DCDC

can be disabled by keeping input power PVDD1 lower than UVLO threshold (7.3V).

- Buck DCDC's Automatic Mode transition: The Buck DCDC will automatically choose PWM mode and PFM mode for higher efficiency at light load. It also provides force PWM mode in the application where really care about supply voltage ripple.
- Buck DCDC's switching frequency: Buck DCDC's typical switching frequency is 450 KHz, with 24KOhm resistor connected on board from Freq_set pin to ground. The switching frequency, Fsw, can also be adjusted by changing the resistor through the following equation:

$$F_{SW} = \frac{1}{R_{set} \times 9 \times 10^{-5}}$$

Fsw is in kHz, Rset is in kΩ.

Also, the Buck DCDC also provides option to select internal resistors to avoid noise coupling on FREQ_SET pin and better fix the frequency. If internal resistor is selected, fixed 450 kHz and 225 kHz options are available.

- Buck DCDC's Current limit: The buck DCDC will limit its output current to be less than 600mA. This feature is added for safety, to protect against output short to ground and problematic current increases which will cause chip and board reliability problems. If load current greater than 600mA is applied to the DCDC output, the buck DCDC will lower down its 3.3V output and will operate as a 600mA current source. Figure 8 shows the inductor current and voltage behavior when 3.3V output is suddenly shorted to ground.

The VDDG LDO is used to set the Vgs output swing for pre-driver, the output voltage can be programmed to be 9V,10V,12V,15V,18V to match different Power FETs.

Figure 6. Buck DCDC's efficiency vs. load current

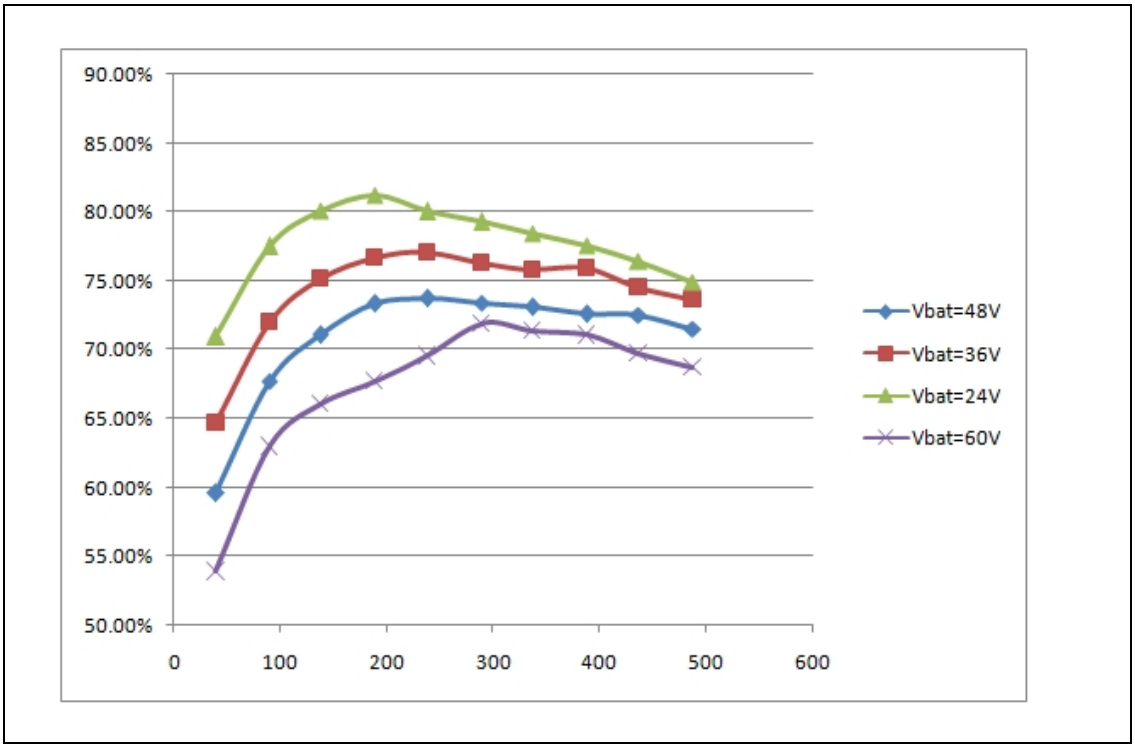


Figure 7. PVDD1=24V, load step 0mA to 400mA to 0mA, 3.3V power waveform in forced PWM mode

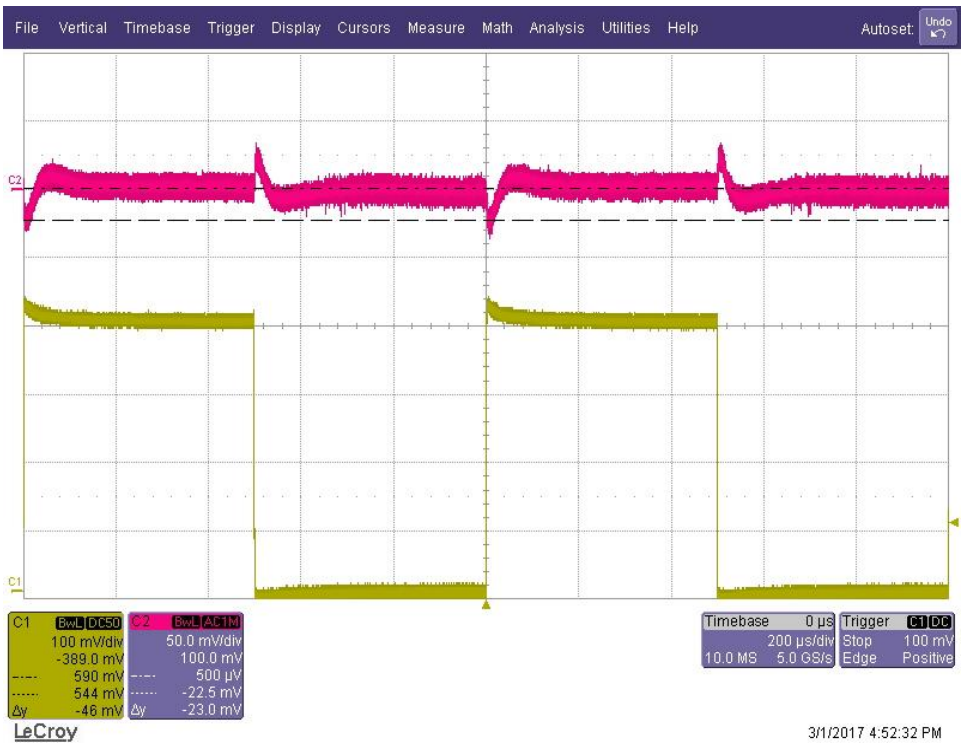
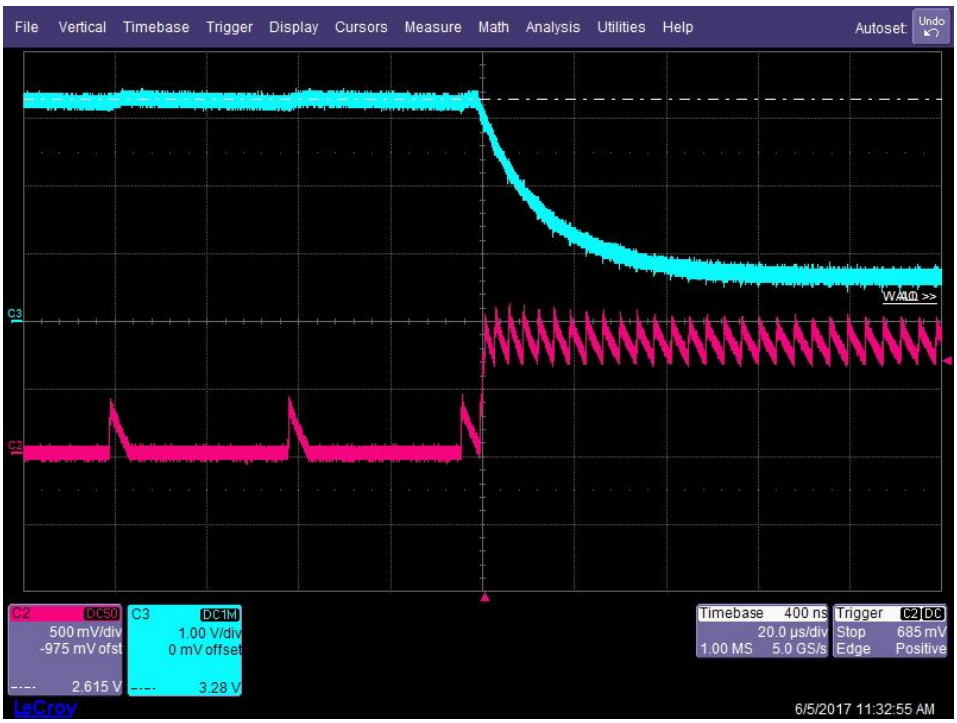


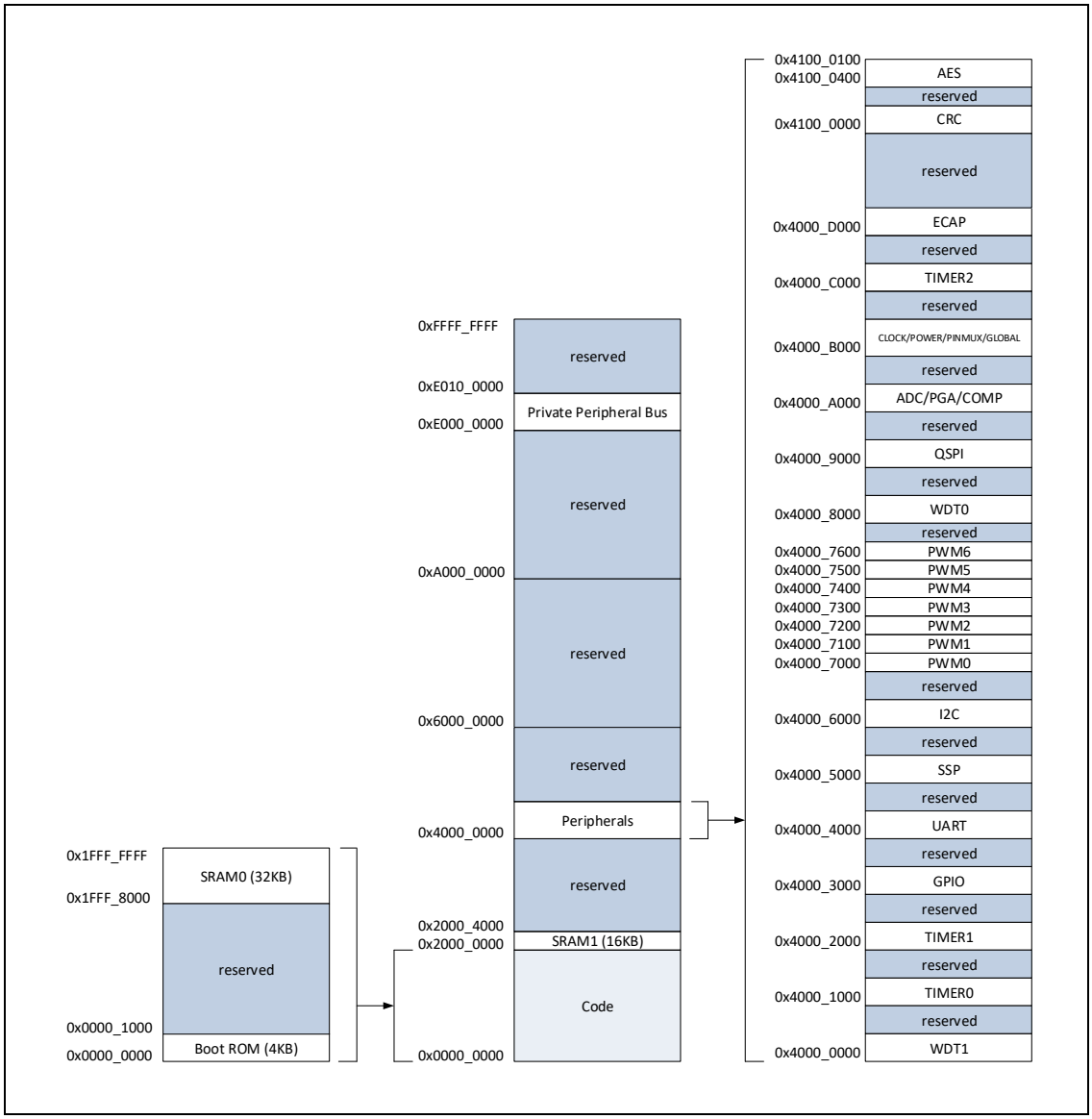
Figure 8. Buck DCDC output and inductor current behavior when 3.3V is hard short to ground



4 Memory mapping

The memory map of SPD1078 is shown in Figure 9.

Figure 9. Memory map



5 Electrical characteristics

5.1 Absolute maximum ratings

Table 2. Absolute maximum ratings (1)(2)

Symbol	Parameter	Min	Max	Unit
V_{DDP0}	Main supply voltage, with respect to V_{SS}	-0.3	63	V
V_{DDP1}	DCDC power supply voltage, with respect to V_{SS}	-0.3	63	V
V_{DDG}	Gate Drive voltage, with respect to V_{SS}	-0.3	18	V
$V_{BOOT\_U/V/W}$	Bootstrap voltage, with respect to V_{SS}	-0.3	76	V
V_{DD}	Supply voltage, with respect to V_{SS}	-0.3	4.6	V
V_{DDA}	Analog voltage, with respect to V_{SSA}	-0.3	4.6	V
V_{IN}	Input voltage (V_{DD} = 3.3 V)	-0.3	4.6	V
V_O	Output voltage	-0.3	4.6	V
I_{IC}	Input clamp current	-20	+20	mA
I_{OC}	Output clamp current	-20	+20	mA
T_J	Junction temperature(3)	-40	+125	°C
T_{stg}	Storage temperature(3)	-65	+150	°C
$T_{retention}$	Flash data retention duration (T_J = 85 °C)	20	-	years

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these is not implied.

(2) All voltage values are with respect to V_{SS}, unless otherwise noted.

(3) Long-term high-temperature storage or extended use at maximum temperature conditions may result in a reduction of overall device life.

5.2 Recommended operating conditions

Table 3. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Nom	Max	Unit
V_{DDP0}	Main power supply	-	8		60	V
V_{DDP1}	Power supply for DCDC	-	7.3		60	V
V_{DD}	Supply voltage	-	2.97	3.3	3.63	V
V_{SS}	Supply ground	-	-	0	-	V
V_{DDA}	Analog supply voltage	-	2.97	3.3	3.63	V
V_{SSA}	Analog ground	-	-	0	-	V
V_{IH}	High-level input voltage	V_{DD} = 3.3 V	2.4	-	V_{DD}+0.3	V
V_{IL}	Low-level input voltage	V_{DD} = 3.3 V	V_{SS}-0.3	-	0.6	V
I_{OH}	High-level output source current	V_{OH} = $V_{OH(MIN)}$	-	-	8	mA
I_{OL}	Low-level output sink current	V_{OL} = $V_{OL(MAX)}$	-	-	3.5	mA
T_J	Junction temperature	-	-40	-	+105	°C

5.3 GPIO Electrical characteristics

Table 4. Electrical characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	High-level output voltage	I_{OH} = I_{OH} MAX	2.6	-	-	V
V_{OL}	Low-level output voltage	I_{OL} = I_{OL} MAX	-	-	0.4	V
I_{IL}	Low-level input current (Pin with pull-up enabled)	V_{DD} = 3.3V, V_{IH} = 0 V	-	-	60	uA
I_{IH}	High-level input current (Pin with pull-up enabled)	V_{DD} = 3.3V, V_{IH} = V_{DD}	-	-	5	uA
I_{OZ}	Output current tri-state (Pin with pull-up disabled)	V_{DD} = 3.3V V_O = V_{DD}/0V	-	-	1	uA

5.4 1.2V internal regulator characteristics

Table 5. 1.2V internal regulator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	2.97	3.3	3.63	V
VCAP12	Output voltage	Light load(1)	1.14	1.2	1.26	V
		Heavy load(2)	1.14	1.2	1.26	V

(1) Light load case = Chip starts up as default.

(2) Heavy load case = Set PLL frequency to 150 MHZ, turn on all PWM modules.

5.5 12-bit ADC characteristics

Table 6. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	2.97	3.3	3.63	V
N_R	Resolution	No missing code. Monotonic	12	-	-	bit
F_S	Conversion speed	-	-	-	4	MSPS
V_{AIN}	Input voltage range	-	0	-	V_{DDA}	V
V_{REF}	Reference voltage	-	1.19	1.2	1.21	V
I_{PAD}	Operational current	V_{DDA} = 3.3 V	-	5.8	6.96	mA
INL	Integral linearity error	-	-3.0	-	3.0	LSB
DNL	Differential linearity	-	-1.0	-	1.0	LSB
E_{OFF}	Offset error	Without calibration	-60	-	60	LSB
E_{GAIN}	Gain error	Without calibration	-120	-	120	LSB
E_{OFF2}	Channel to channel offset	-	-4	-	4	LSB
E_{GAIN2}	Channel to channel gain error	-	-30	-	30	LSB
T_{COEF}	ADC temperature coefficient with internal reference	-	-	30	-	ppm/°C
T_{PWRUP}	Power-up time	-	-	-	200	us
SNR	Signal-to-noise ratio	Fin = 10 kHz, Amp = 0.94F_S, N = 8192	-	65.0	-	dB
THD	Total harmonic distortion		-	76.6	-	dB
ENOB	Effective number of bits		-	10.5	-	bit
SFDR	Spurious free dynamic range		-	79.6	-	dB
T_{SLOPE}	Degrees C of temperature movement per measure ADC LSB change of the temperature sensor	-	-	3.8473	-	°C/LSB
T_{OFFSET}	ADC output at 50 °C of the temperature sensor	-	-	4182	-	LSB

5.6 PGA characteristics

Table 7. PGA characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	2.97	3.3	3.63	V
V_{AIN}	Input voltage range	-	0	-	V_{DDA}	V
V_{OUT}	Output voltage range	-	0.4	-	V_{DDA}-0.4	V
R_{IN}	Input impedance	-	-	Hi-Z	-	Ω
G	Gain	Single-ended mode	2, 4, 8, 16			-
		Differential mode	4, 8, 16, 32			-
E_{GAIN}	Gain error	G = 2, Single-ended mode	-1.50	-	1.50	%
		G = 16, Single-ended mode	-4.00	-	4.00	%
V_{OS}	Offset	-	-15	-	15	mV
T_{SETTLE}	Settle time	G = 2, Single-ended mode	-	-	388	ns
		G = 16, Single-ended mode	-	-	500	ns
I	Current consumption	Only one PGA	-	400	700	uA

5.7 Analog comparator characteristics

Table 8. Analog comparator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	2.97	3.3	3.63	V
V_{OFFSET}	Offset voltage	-	-15	-	15	mV
V_{HYST}	Hysteresis voltage	-	-60	-	60	mV
T_D	Delay time – comparator response time to PWM shunt down (Asynchronous)	-	-	40	-	ns

5.8 Internal DAC characteristics

Table 9. Internal DAC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	2.97	3.3	3.63	V
N_{CM}	Current mode resolution	Monotonic, no missing code	10	-	-	bit
V_{FS}	Full scale value	Operating in current mode with double range option	1.84	-	2.70	V
DNL	Differential linearity	-	-1	-	1	LSB
INL	Integral linearity	-	-3	-	3	LSB
E_{OFF}	Offset error	-	-50	-	50	mV
N_{VM}	Voltage mode resolution	Monotonic, no missing code	7	-	-	bit
T_{SETTLE}	DAC settling time	Design guarantee	-	10	-	us

5.9 Flash memory characteristics

The characteristics are given at T_J = -40 to 105 °C unless otherwise specified.

Table 10. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{BP1}	Byte program time (first byte)(1)	-	-	15	30	us
t_{BP2}	Additional byte program time (after first byte)(1)	-	-	2.5	5	us
t_{PP}	Page program time	-	-	0.4	0.8	ms
t_{SE}	Sector erase time (4KB)	-	-	30	300	ms
t_{BE1}	Block erase time (32KB)	-	-	120	800	ms
t_{BE2}	Block erase time (64KB)	-	-	150	1000	ms
t_{CE}	Chip erase time	-	-	1	4	s
N_{END}	Endurance (erase/write cycle)	-	100k	-	-	cycles
t_{RET}	Data retention duration	T_J = 85 °C	20	-	-	years

(1) For multiple bytes after first byte within a page, $t_{BPN} = t_{BP1} + t_{BP2} * N$ (typical) and $t_{BPN} = t_{BP1} + t_{BP2} * N$ (max), where N = number of bytes programmed.

5.10 Electrical sensitivity characteristics

Table 11. ESD absolute maximum ratings

Symbol	Parameter	Conditions		Max	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human Body Model)	Ambient temperature T_A = 25 °C		2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (Charge Device Model)	Ambient temperature T_A = 25 °C	-	500	V
			Corner Pin	750	V

Table 12. Electrical sensitivities

Symbol	Parameter	Conditions	Max	Unit
LU	Static latch-up	Ambient temperature T_A = 85 °C V_{DD} = 3.63V, VCAP12 = 1.32V	100	mA

5.11 DCDC switching regulator characteristics

Table 13. DCDC switching regulator characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
PVDD1	Input Supply voltage	-	7.3	-	60	V
$PVDD1_{UVT}$	PVDD1 under voltage trigger threshold	-	-	7.3	-	V
$PVDD1_{UVR}$	PVDD1 under voltage release threshold	-	-	7.68	-	V
VDD_{DCDC}	DC/DC output voltage	-	3.15	3.3	3.45	V
F_{SW}	DC/DC Switching Frequency	Select internal resistor	360	420	483	kHz
R_{DSON_HS}	DC/DC high side Ron	-	-	1.6	-	Ω
R_{DSON_LS}	DC/DC low side Ron	-	-	1.3	-	Ω
η	Efficiency	PVDD1=24V, 200mA load	-	81	-	%
I_{limit}	Current limit threshold	-	-	600	-	mA
T_{SS}	DC/DC Start up time	-	-	820	-	us

5.12 Pre-Driver characteristics

Table 14. Pre-Driver characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
PVDD0	Input Supply voltage	-	8	-	60	V
D_{MAX}	Maximum supported duty cycle	Charge pump will replenish bootstrap capacitor when high side is turned on	-	100	-	%
T_{DR}	Rising edge propagation delay	1nF Capacitor as load	-	40	-	ns
T_{DF}	Falling edge propagation delay	1nF Capacitor as load	-	40	-	ns
VPX_{MIN}	High side return ground Minimum	Min voltage where high side signal still propagate	-10	-	-	V
$I_{SourceMax}$	Pre-Driver Max sourcing capability	1A/2A programmable	-	2	-	A
$I_{SinkMax}$	Pre-Driver Max sinking capability	1A/2A programmable	-	2	-	A

5.13 12V linear regulator characteristics

Table 15. 12V linear regulator characteristics

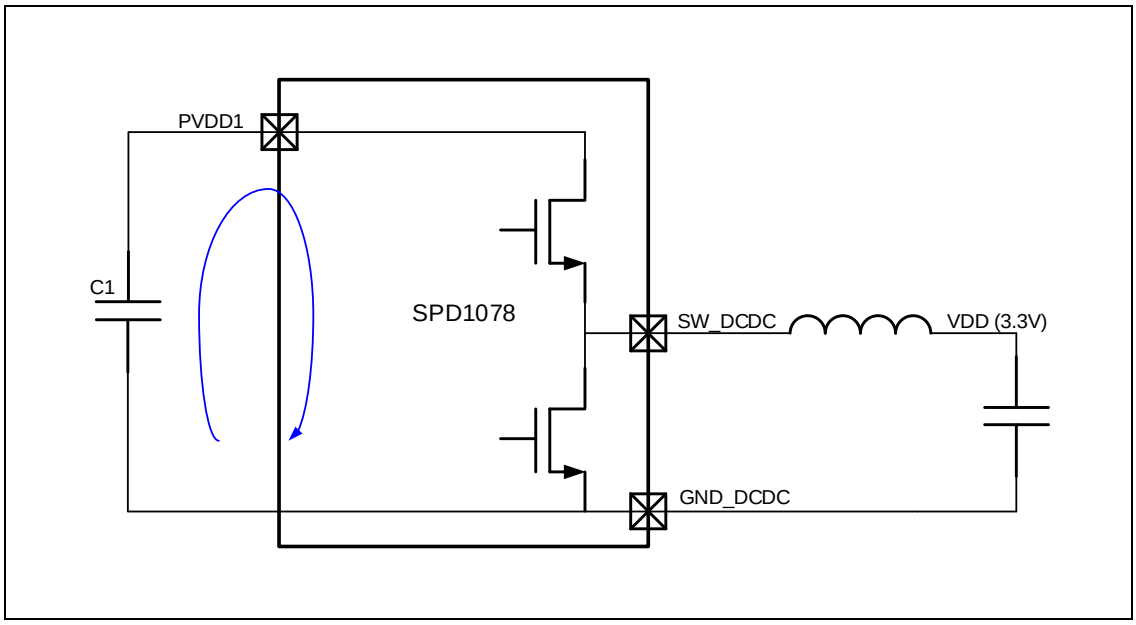
Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
VDDG	Pre-Driver swing voltage	9V, 10V, 12V, 15V, 18V programmable	11.4	12	12.6	V
I_{VDDG_Limit}	LDO current limit	-	-	80	-	mA

6 PCB layout guidance

6.1 Power management considerations

- GND_DCDC and VSS should be well connected by Copper plate on PCB board.
- Decoupling capacitance C1 should be put as close as possible to PVDD1 pin to minimize the current loop area shown in Figure 10. 2.2uF ceramic cap is recommended.
- Minimize the routing on SW_DCDC pin to the inductor, in order to reduce the parasitic resistance and capacitance.
- Output capacitor should be put close to the inductor, and the ground connection should be tied to IC ground VSS through short trace or copper plate.
- Enough through holes should be put under the chip EPAD for a good connection to the copper ground plate. This is essential for thermal dissipation.
- SW_DCDC and BOOT_DCDC are power switching pins with swing amplitude of PVDD value, so sensitive analog traces or pins, like Freq_set, on PCB should be put as far as possible from these 2 signals.
- FB_DCDC is the feedback signal for buck control loop, it should be put away from noisy devices such as inductor.

Figure 10. Simplified buck DCDC diagram

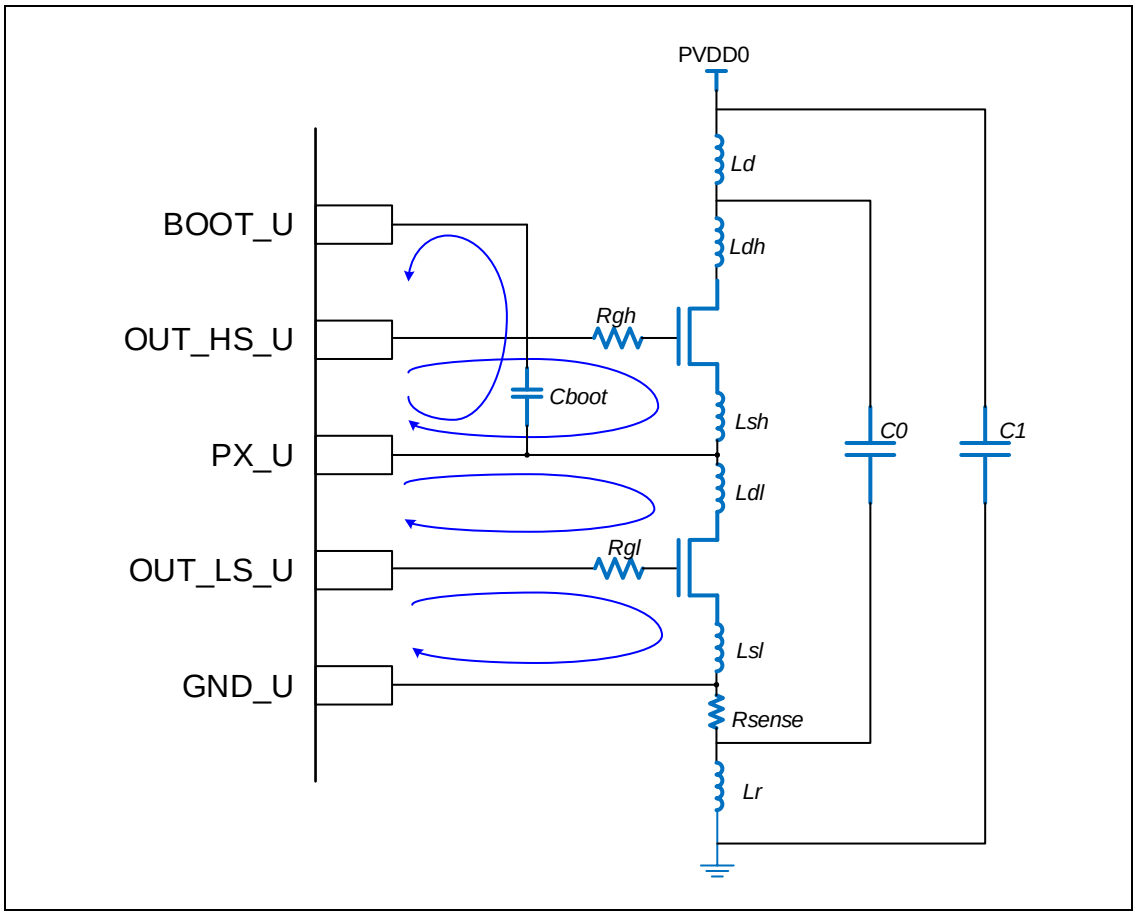


6.2 Pre-Driver considerations

- Co-locate power FET pairs with drain of low-side adjacent to source of high-side to minimize both Lsh and Ldl, and pairs placed close to each other to reduce routing distance and minimize Lr and Ld.
- Use thick, direct tracks between FET's with no loops or deviation.

- Minimize the areas of major current paths shown by arrows in the diagram of Figure 11 to avoid any loops.
- Avoid interconnect vias as they add significant inductance.
- In case of standing power FET's, reduce the effect of lead inductances by lowering package height above PCB.
- Connect VS_LOW to the very tip of low-side FET source, to minimize Lsl. For the same reason, connect Rsense as close as possible to low-side FET source and C0 right at the other end of Rsense.
- Connect the other end of C0 (shown in Figure 11) as close as possible to the drain of high-side FET, in order to provide the lowest-parasitic return path for current.
- Place pre-driver IC closer to power switches; route gate driver control signals HSO and LSO, and high- and low-side return grounds VPX and VS_LOW with straight as-short-as-possible traces.
- Connect bootstrap capacitor as close as possible to VPX and VBOOT pins.
- Connect low-ESR bypass capacitors from PVDD, VDDG, VCP to ground, placing capacitors as close as possible to their respective pins, with the other end of each capacitor having a strong connection to board ground.
- Use power FET's with fast body diode turn-on times and as small as possible diode reverse charges.

Figure 11. Simplified Pre-Driver diagram



(1) This figure shows the Pre-Driver U-phase circuit diagram. And the Pre-Driver V-phase and W-phase circuit diagrams are the same.

6.3 Example layout

A possible illustration of board layout is given in Figure 12. Note the worst-case parasitic is phase W, because it has longest routing to the main power input electrolytic capacitor, and one of the longest routing paths from pre-driver SPD1078 to its' FET input and ground returns VPX_W and VS_LOW_W. The top and bottom photos of an example board are also shown in Figure 13.

A few other important board design concepts are shown in Figure 12. First of all, diodes may be added across resistors Rgh and Rgl. While the resistors allow slow charging of power FET's, diodes shunt resistors and allow fast discharging of power FET's. This may help preventing crow-bar current, as current via drain-to-gate capacitance of power FET is shunted via the respective diode and prevents turn-on of the power FET. The diodes across gate resistors should be fast turn-on with low forward bias; typically Schottky diodes may be also used. In order to slow down charging and discharging of power FET's, and in order to provide a shunt path across gate-source terminals when the FET is off, a small low-ESR capacitor across gate-source may be added. If used, this capacitor is typically from few tens to few hundreds of pF.

Furthermore, very heavy negative switching spike on VPX can also drag VBOOT below ground by more than diode forward voltage (via Cboot). This, however, will turn on the p-n diode present on-chip, which results in large current injection on-chip. This in turn may cause latchup or other chip mis-operation and thus should be avoided.

To suppress Vboot spiking far below ground, a small resistor Rboot may be added in series with Cboot. The resistor cannot be too large, or it will make Cboot ineffective, which will result in large transient VBOOT-to-VS_LOW voltage and damage pre-driver. Typically, if ever used, the Rboot resistor is between 2 and 10Ω. As alternative to Rboot, resistor Rsh may be used. The resistor Rsh is not only in series with Cboot, but also serves as a series resistor when charging/discharging the high-side FET, performing functions similar to Rgh.

Similarly, Rsl performs functions similar to Rgl. In addition, Rgl attenuates any inductive ripple which occurs at the source of low-side power FET as seen by VS_LOW of pre-driver.

To suppress transient VPX negative spike, a diode Dclamp from board ground to VPX may also be added. Dclamp should be fast turn-on diode with low forward bias.

Figure 12. Example layout

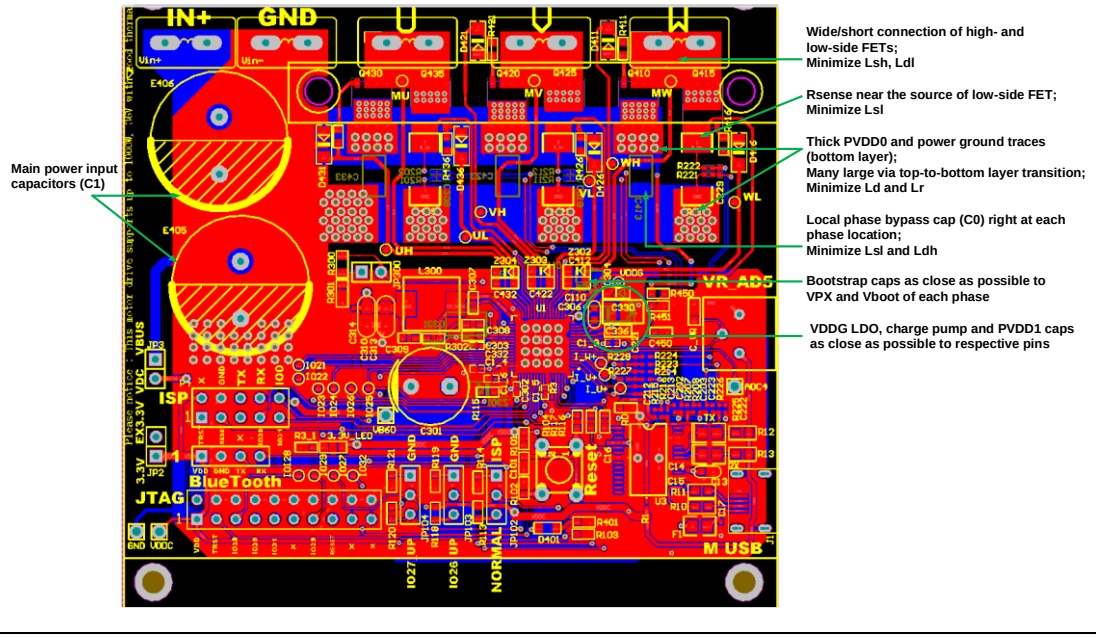
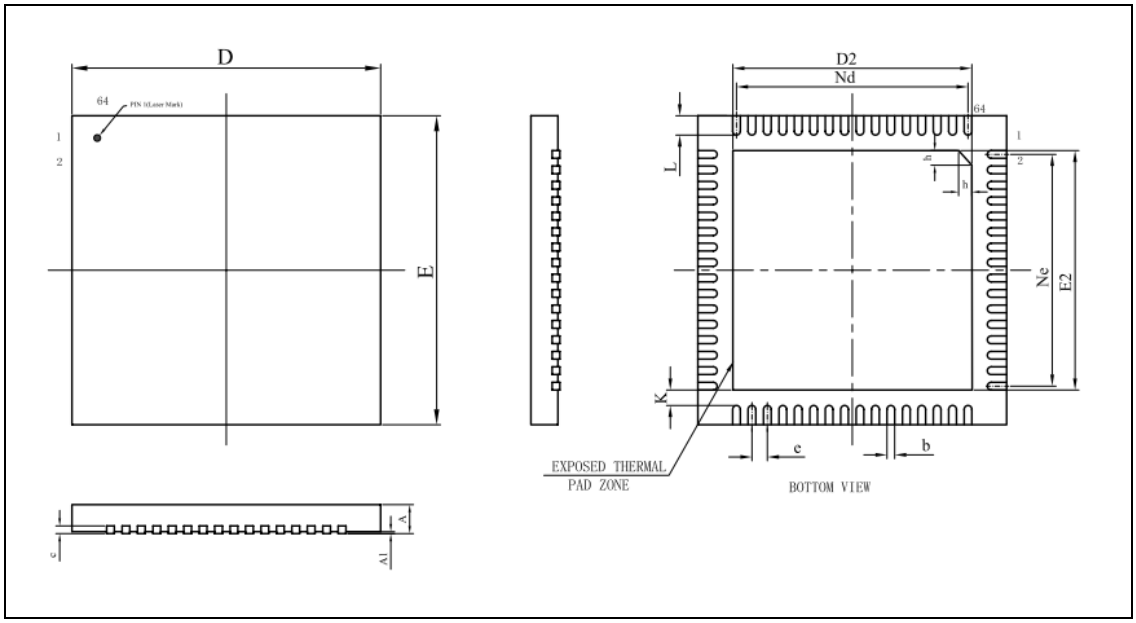


Figure 13. Board photo

7 Package information

The package type of SPD1078 is 64-pin QFN. The detail information is as follows:

Figure 14. QFN64L pin, 8 x 8 mm package outline



(1) Drawing is not to scale.

Table 16. QFN64 – 64 pin, 8 X 8 mm thin quad flat package mechanical data

SYMBOL	MILLMETER		
	MIN	NOM	MAX
A	0.7	0.75	0.8
A1	--	0.02	0.05
b	0.15	0.2	0.25
c	0.18	0.2	0.25
D	7.9	8	8.1
D2	6.1	6.2	6.3
e	0.40BSC		
Nd	6.00BSC		
E	7.9	8	8.1
E2	6.1	6.2	6.3
Ne	6.00BSC		
L	0.45	0.5	0.55
K	0.2	--	--
h	0.3	0.35	0.4

8 Revision history

Table 17. Document revision history

Date	Revision	Changes
19-Sep-2017	1	Initial release.
25-Oct-2017	2	1. Updates Figure 5. SPD1078 typical application diagram. 2. Updates Figure 10. Simplified buck DCDC diagram. 3. Updates Figure 11. Simplified Pre-Driver diagram. 4. Updates Figure 12. Example layout.
08-Jun-2018	3	1. Updates Fsw equation in Section 3.25.
20-Jun-2018	4	1. Modifies Table 2. Absolute maximum ratings (1)(2).
28-Jun-2018	5	1. Modifies Table 3. Recommended operating conditions.
20-Dec-2018	6	1. Modifies Table 2. Absolute maximum ratings (1)(2).
15-Aug-2019	7	1. Modifies JTAG and RESETn pin description in Table 1.SPD1078 pin definitions. 2. Updates Table 3. Recommended operating conditions. 3. Updates Table 4. Electrical characteristics.
20-Dec-2019	8	1. Add Table 10. Flash memory characteristics. 2. Add Table 11. ESD absolute maximum ratings. 3. Add Table 12. Electrical sensitivities.
27-May-2021	9	1. Update Figure 4. SPD1078 QFN64L pin-out.