Application Note

Addressing Thermal Issues in Pre-Driver of SPD11xx Product Family

Revision 1 – May 2020

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1 Pre-Driver overview

Pre-Driver is designed to drive the power FET's, which in turn drive various inductive loads, such as motor phases, reactive power supply components and so on. A simplified 3-phase U/V/W Pre-Driver system is shown in Figure 1-1. The inductive load is driven by a half-bridge phase consisting of low-side power FET NLO and high-side power FET NHI. The figure depicts a three-phase system, having three half-bridge power FET pairs, phases conventionally named U, V, and W.

The Pre-Driver on-chip components include the low-voltage PWM inputs PWM_LO (for low-side) and PWM_HI (for high-side). The low-voltage is typically 3.3 or 5V. The PWM_LO inputs are converted to the Pre-Driver gate voltage level (VDDG) in the range of 10 to 15V to drive the low-side outputs OUTL which in turn are coupled to the gates of low-side power FET's NLO. The voltage VDDG is supplied by a voltage regulator, a switching power converter or LDO. Spintrol allows using both on-chip VDDG regulator and (if it is necessary to reduce chip self-heating) off-chip VDDG regulator.

The high-side Pre-Driver path couples the output OUTH to the gate of the high-side power FET NHI. Just like low-side signal OUTL, OUTH range is also around 10 to 15V. However, while OUTL signal range is with respect to ground GND, the high-side signal OUTH is with respect to the floating high-side ground VPX. The high-side ground is actually the motor switching node VPX which is connected to the source of the high-side power FET NHI. The input PWM_HI signal is level shifted by noise-resistant level shifter LSH into the VBOOT/VPX domain. The bootstrap capacitor Cboot supplies the charge to the high-side Pre-Driver which drives NHI during switching of the phase. The bootstrap capacitor charge is replenished via bootstrap diode D when high-side is off, low-side is on (VPX close to zero). It is drawn from the low-side power rail VDDG capacitor C_VDDG, which is larger than Cboot. For example, most common recommended value for Cboot is 100nF, while C_VDDG is recommended to be 2.2uF. When VPX is close to zero, VBOOT cannot drop below VDDG-0.7V due to bootstrap diode D which maintains the charge across Cboot. When the high-side is on, a built-in charge pump CHP maintains the gate-to-source voltage of NHI (voltage across respective Cboot) close to VDDG level.

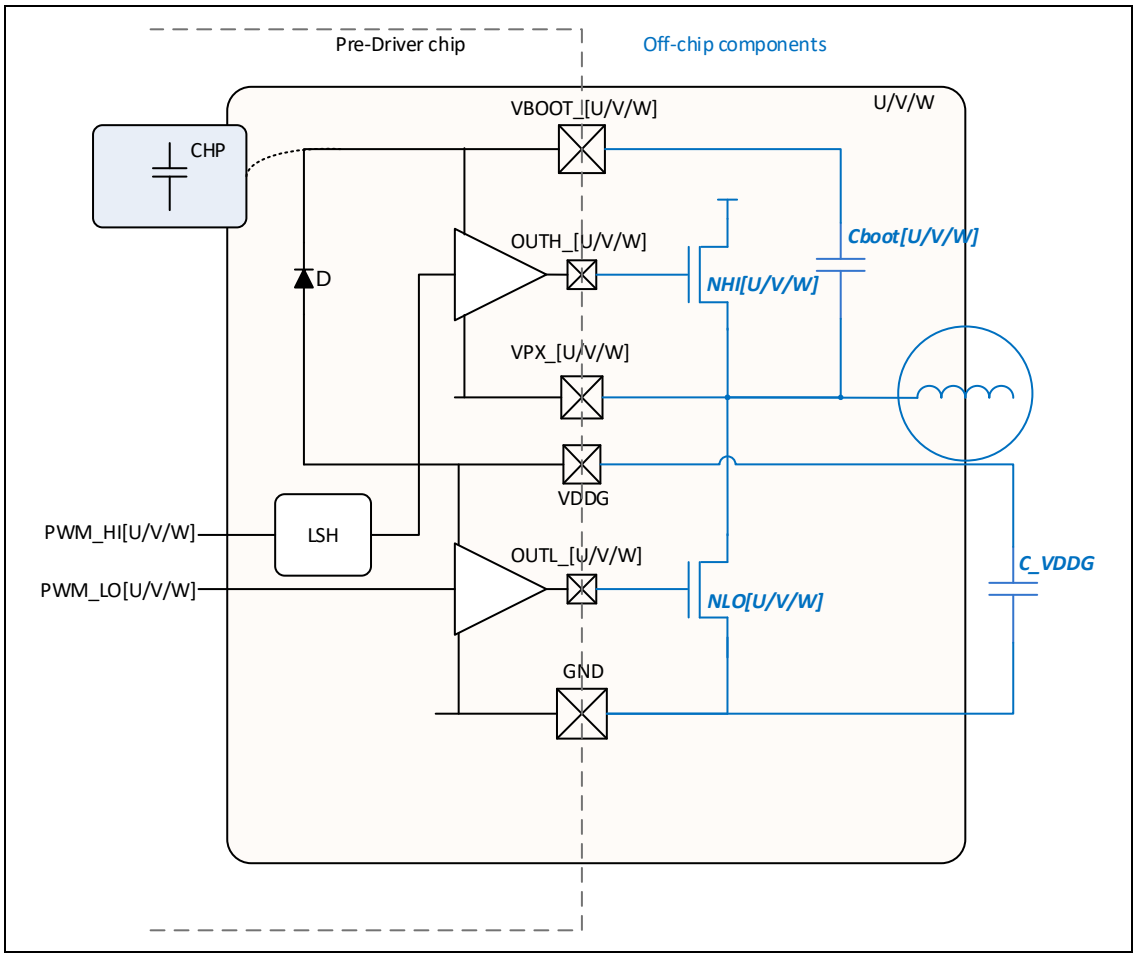
There are two key features worth noting about a Pre-Driver. First, low- and high-side must operate with non-overlap. In addition to non-overlap implemented in PWM_LO and PWM_HI inputs to Pre-Driver, internal non-overlap is implemented for safety. Second, Pre-Driver operation must start with low-side pulse. This guarantees that a proper voltage across Cboot capacitor is established before high-side is turned on, in order to avoid malfunction and even damage of the circuit. In a conventional Pre-Driver, a resistor is required in series with bootstrap diode D, in order to limit diode current during the first pulse or in case of large voltage loss on Cboot. Spintrol's Pre-Drivers discussed in the application note do not have this requirement, because the current through the diode is clamped by internal safety circuit. At startup, before high side is on, in order to guarantee initial charge on Cboot, the low-side pulse duration must be no less than V(VDDG) x Cboot / 200mA, where 200mA is typical current in the bootstrap diode D path. For example, for V(VDDG)=12V, Cboot=100nF, the initial low-side pulse must be 12 V x 100e-9 F / 200e-3 A=6 s.

Cboot must be chosen to be much larger than the FET input capacitance. The FET input capacitance is usually listed in the datasheet, or it can be estimated from the ratio of gate charge QGG and VDDG. If VDDG=12V, then assuming QGG=36nC we get FET input capacitance Ciss 36nC/12V=3nF. Assuming

Cboot=100nF, voltage loss during bootstrap is 12V x Ciss / (Cboot + Ciss) = 350mV. As a rule of thumb, Cboot should be greater than 10 Ciss.

Finally, conventional bootstrap architecture utilizing floating power VBOOT with a holding capacitor Cboot has a limitation of maximum on-time. This is because when high side is on, the current off VBOOT terminal discharges Cboot and destroys the voltage headroom for high-side VBOOT/VPX circuitry in the Pre-Driver. In case of Spintrol Pre-Drivers described in this application note, a charge pump is introduced which replenishes charge on Cboot when high-side is on. Therefore, high-side can be on indefinitely and 100% duty cycle is allowed.

Figure 1-1:A simplified 3-phase Pre-Driver arrangement



2 Pre-Driver power dissipation impact and reduction

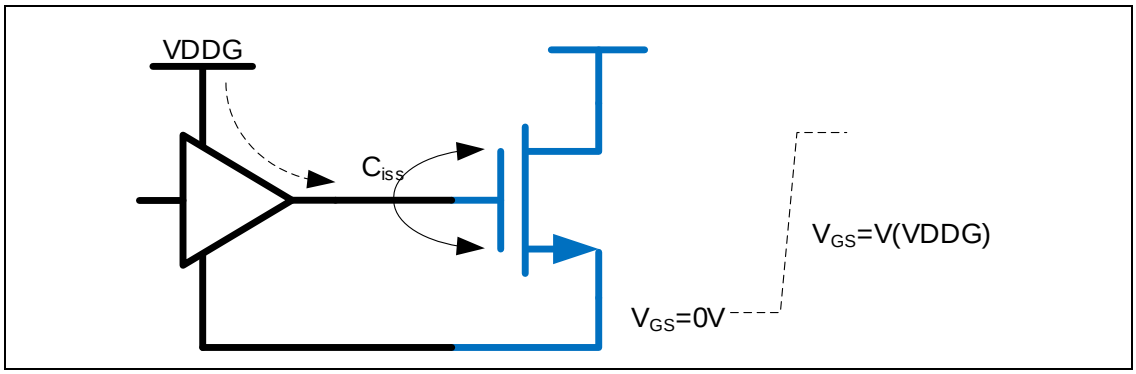
2.1 Pre-Driver power dissipation calculation

The main current supplied by Pre-Driver is the current charging the external power FET. As shown in Figure 2-1, when the power FET is charged to a voltage V_{GS}, the total charge is equal to:

$$Q_G = V_{GS} \cdot C_{iss} = V(VDDG) \cdot (C_{gs} + C_{gd})$$

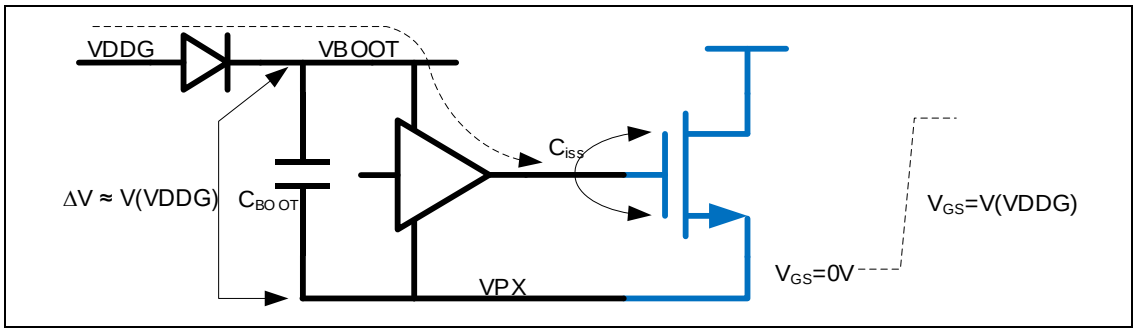
Here, Ciss denotes input capacitance equal to the sum of gate-source and gate-drain capacitances. It is a standard parameter listed in FET datasheets. For the high-side FET the voltage V_{GS} may be a little smaller than V(VDDG) because of bootstrap diode forward voltage drop and because of charge sharing between Cboot and Ciss during bootstrap process. But as we noted before, one must choose Cboot >> Ciss and the diode drop is less than 0.7V, so we will neglect the effect for the sake of simplicity.

Figure 2-1:Pre-Driver low side charging power FET from zero to approximately V(VDDG)



It is very important to realize that not only for low side, but also for high side the current comes from the supply VDDG. This is because (referring to Figure 2-2) the current comes from capacitor Cboot, and the capacitor itself is charged when low-side is on via bootstrap diode D, as depicted in Figure 1-1.

Figure 2-2:Pre-Driver high side charging power FET from zero to approximately V(VDDG)



For a three-phase half-bridge topology driving a single motor there are six power FET's. Therefore, the total current provided by Pre-Driver for charging/discharging power FET's is equal to:

$$I_{FET} = 6 \cdot Q_G \cdot f = 6 \cdot V(VDDG) \cdot C_{iss} \cdot f$$

If VDDG is supported by on-chip LDO from input battery voltage pin VBAT, then total power dissipated due to charging/discharging power FET's is equal to:

$$P_{FET} = V(V_{BAT}) \cdot 6 \cdot Q_G \cdot f = V(V_{BAT}) \cdot 6 \cdot V(VDDG) \cdot C_{iss} \cdot f$$

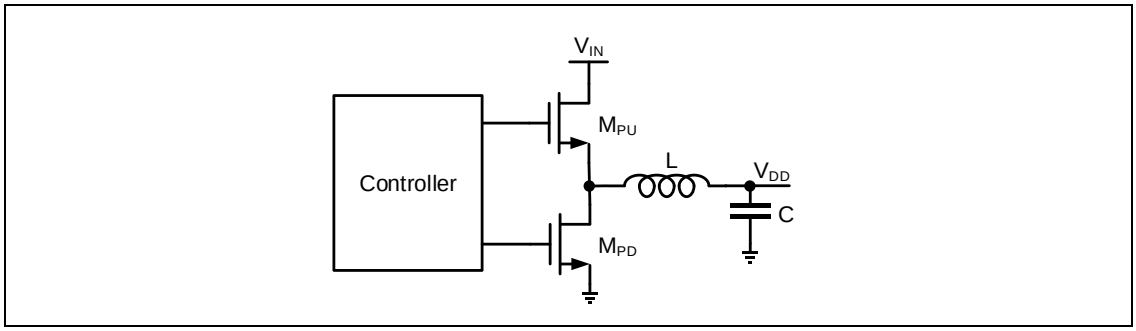
Putting in some numbers, for V(VBAT)=24V, Ciss=15nF, f=30KHz and VDDG=12V, we can get P_{FET}=0.775W. This is a substantial component of overall power dissipation. In addition, the MCU working off 3.3V supply will dissipate between 50 to 100mA, which assuming 80mA translates to the power of 0.264W, and internal Pre-Driver circuits will dissipate 3 or 4 mA from VBAT directly to ground, which will dissipate roughly 0.16W. In total, we can estimate the power to be approximately 1.2W.

As a rule of thumb, good board designs using Spintrol's QFN-based products can have thermal resistance as low as 40 °C/W. Then 1.2W will cause as much as 48 degrees heating of the chip. Such power dissipation will cause prohibitive heating of the chip. Note that we did not include power dissipated in the VBAT to 3.3V Buck as it is delivered to the MCU, as it is done in SPD1148 or SPD1078.

2.2 Buck power dissipation calculation

Figure 2-3 shows a step-down Buck regulator. The Buck regulator consists of a driving stage having pull-up and pull-down transistors M_{PU} and M_{PD}, controller, and LC filter which filters output of the driving stage V_{SW} to deliver power V_{DD} to the load. While M_{PU} and M_{PD} drive the switching node V_{SW} from roughly ground to input power level $V(V_{IN})$, controller senses V_{DD} and sometimes inductor current and controls the rate of M_{PU}/M_{PD} switching to ensure Buck output V_{DD} is equal to the desired value.

Figure 2-3:Step-down Buck regulator



The efficiency η of Buck regulator is defined as the ratio of power delivered to the load to the total power taken from the input, i.e.

$$\eta = \frac{P_{LOAD}}{P_{total}} = \frac{V(V_{DD}) \cdot I_{DD}}{V(V_{IN}) \cdot I_{IN}}$$

Here, I_{DD} and I_{IN} are current delivered to the load and current out of V_{IN} respectively.

Typical power converters have their efficiencies in the range between 85 and 90%. Efficiency drops at low current loads, but low current loads are not of interest in this application note as we are focusing on thermal performance which is of concern at high current loads. Efficiency numbers are usually listed at by the Buck regulator providers; here we will assume η=85%.

Since many SPD1xxx products use embedded Buck regulators, the power dissipated in the Buck regulator and power dissipated in the load have to be added up as it is dissipated in the same semiconductor package. Here we assume that power delivered to V_{DD} is dissipated mostly in the chip and not in on-board elements. For example, in SPD1148, all power delivered to 3.3V supply DVDD is dissipated in the MCU as compared to on-board resistors connected to DVDD supply.

Usually, I_{IN} is unknown. However, the load current is known (here denoted I_{DD}). As an example, putting in typical numbers already discussed in the previous chapter as $V(V_{IN})$=24V, I_{DD}=80mA, $V(V_{DD})$=3.3V we can get:

$$P_{total} = V(V_{IN}) \cdot I_{IN} = \frac{V(V_{DD}) \cdot I_{DD}}{\eta} = 0.31W$$

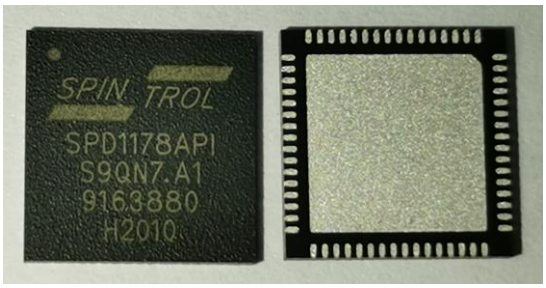
Note that if LDO (and not Buck) was used to provide current to V_{DD}, then the power would have been $V(V_{IN})$ x I_{DD}=1.92W, a much larger number.

When calculating power dissipated in a chip, it is necessary to understand how the power is delivered in the system. For example, in SPD1078 and SPD1148 DVDD is derived from VBAT to DVDD by Buck (V_{IN}=VBAT, V_{DD}=DVDD) and VDDG is derived by LDO from VBAT to VDDG. In SPD1188 VDDG is derived by Buck from VBAT to VDDG (V_{IN}=VBAT, V_{DD}=VDDG) and DVDD is derived by Buck from VDDG to DVDD (V_{IN}=VDDG, V_{DD}=DVDD). In SPD1178, DVDD is supplied externally while VDDG is derived by LDO from VBAT to VDDG.

3 Improving thermal performance via layout

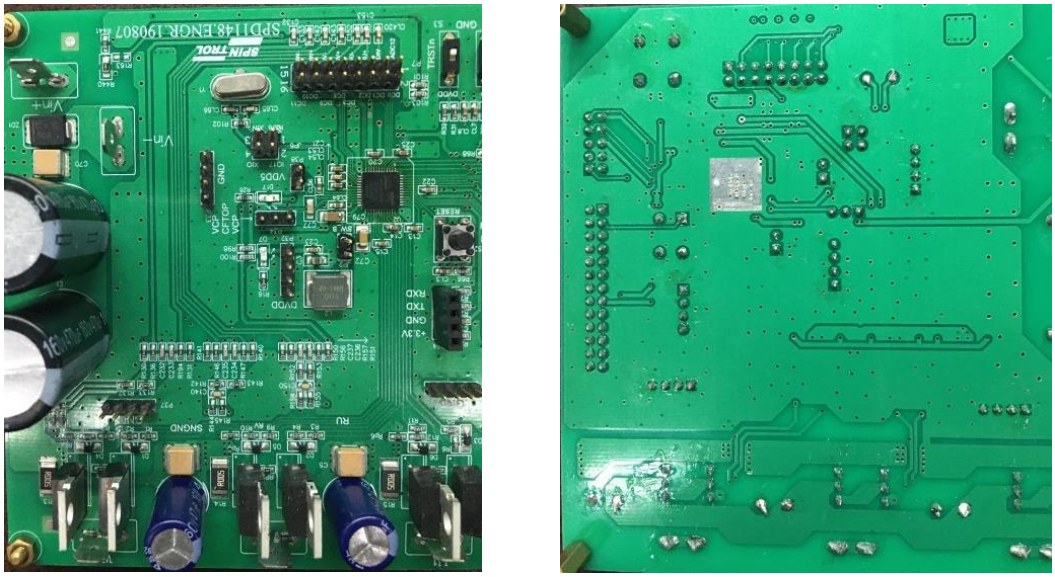
Spintrol's products containing Pre-Driver come in QFN package. One such package is shown in Figure 3-1. As can be seen, the pads are on all four sides of the package. The package has a large exposed pad (EPAD) that is bonded to the bottom of silicon die and should be electrically connected to ground. Heat generated in the silicon die during operation is removed primarily via EPAD, and care should be taken when designing a board to provide proper heat removal from EPAD to outside. A matching exposed Cu pad has to be laid out on the board for good EPAD soldering. For large EPAD's care should be taken to avoid solder voiding or device lift-up due to non-uniform solder distribution. For proper techniques, board manufacturers and packaging houses should be consulted.

Figure 3-1:QFN package top and bottom view



In order to effectively remove heat from the chip, thermal vias should be used to transfer heat from top level on board to the bottom and then spread out heat as much as possible using bottom layer ground plane. Thermal vias are best in diameter is large, but excessively large diameter can lead to chip soldering issues. For proper sizing of thermal vias board manufacturer and package house should be consulted. It is recommended to place as many thermal vias on the top board metal pad which is soldered to EPAD as reliably possible. The lower level ground plane connected to thermal vias must be laid out to spread out as much as possible so as to spread the heat away and out. Whenever possible, the lower level ground plane should be doubled up in empty top areas, also strapped by thermal vias and thermal via stacks. It is helpful to expose e-pad on the opposite side of the board, making the exposed size pad as large as possible and drilling to it with thermal via stacks, to maximize heat out-diffusion. This is shown in Figure 3-2, where top and bottom of a board is depicted, including the exposed board bottom.

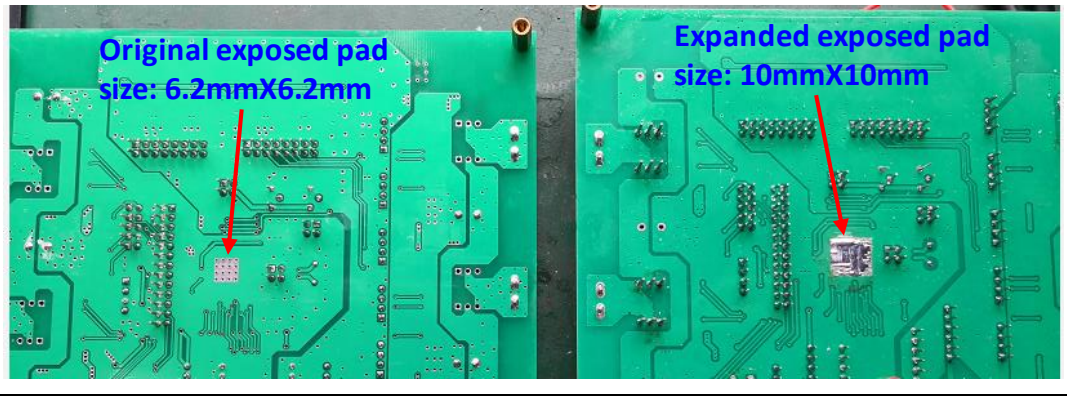
Figure 3-2:Top and bottom view of the board



In addition to adding thermal vias for the Pre-Driver chip, add them for power FET's and nearby high-current areas if necessary. To avoid additional heating and improve reliability, high-current powers and nets should be laid out as wide as possible. Finally, to avoid current crowding and heating, signal and power traces, especially ones conducting large currents, should employ 45° angle rounding; avoid 90° corners.

To emphasize the importance of the exposed bottom pad impact on thermal resistance, the two SPD1178 boards with different sizes of exposed pads were compared. This is shown in Figure 3-3, as the bottom sides of the two boards are displayed side-by-side. The thermal resistance was measured and compared for samples from each board. The board on the left measured 55 °C/W, while the board on the right measured a substantially lower value of 41 °C/W, a more than 25% improvement!

Figure 3-3:Bottom view of two boards with different sizes of exposed pads



In addition to adding thermal vias for the Pre-Driver chip, having thick and wide and possibly exposed lines conducting power/ground or high-current motor output signals from power FET's, as well as adding thermal release paths for power FET's greatly improves thermal performance of a product.

4 Saving LDO power – adding external Buck regulator

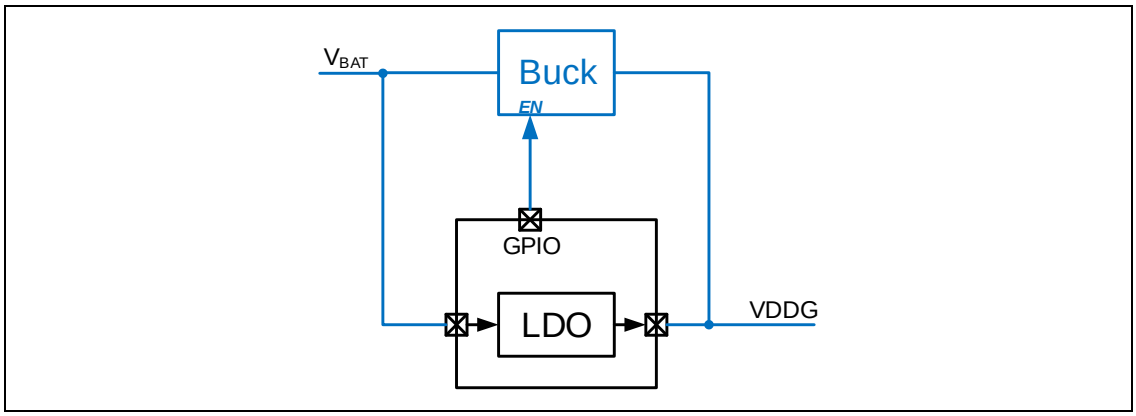
The advantage of LDO as opposed to switching Buck regulator is simplicity, low cost, essentially zero extra pin count and absence of inductors. LDO's, however, suffer from a worse power dissipation problem. This is because while LDO's step down voltage from V_{IN} to V_{DD} (referring to the terminology of Figure 2-3), VDD's current essentially uses V_{IN} for power calculation. When using the LDO (using assumptions of Section 2.2), total power dissipated is:

$$P_{total} = V(V_{IN}) \cdot I_{VDD} = 24V \cdot 80mA = 1.92W$$

Here we put in numbers used in Buck calculations of Figure 2-3 and neglect LDO's own quiescent current which is much smaller than current delivered to V_{DD}. We see that for LDO power dissipation is much higher than for Buck converter and is prohibitive in this given example of a very high current of 80mA.

The products SPD1078, SPD1148, SPD1178 contain on-chip VBAT to VDDG LDO which supplies current to the Pre-Driver. In rare cases of very high-frequency high-performance motor applications at high input battery voltage levels the power dissipation in this LDO can significantly add to the power dissipation of the chip leading to prohibitive chip heating. In this case, VDDG LDO can be substituted by Buck and will be described below.

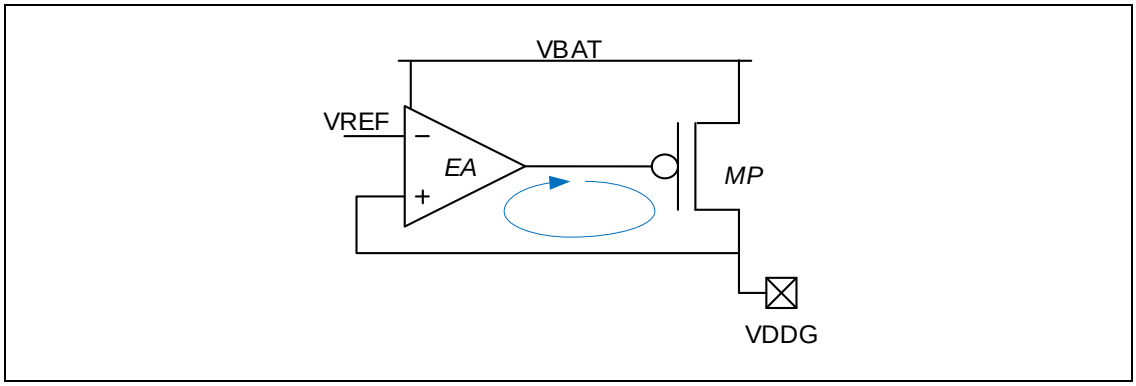
Figure 4-1:Illustration of on-chip LDO and on-board Buck connected in parallel



As shown in Figure 4-1, a Buck DC/DC converter is connected in parallel with the on-chip VDDG LDO. As chip powers up, Pre-Driver is disabled, so is the LDO. The Buck can be hardwired to output VDDG right after VBAT power-up, or it can be enabled by MCU using 3.3V signal output by the chip's General Purpose I/O (GPIO). In the first case, when Pre-Driver is not enabled for VDDG=12V will consume additional 310uA. In the latter case, this current does not constitute additional dissipation because Buck can be enabled right before Pre-Driver is enabled. Note that no matter what kind of Buck scheme is used, the user must guarantee that VDDG comes out after VBAT.

In order to make sure LDO does not fight with Buck regulator, first program LDO voltage to be below Buck voltage (write to register LDOGCTL). This must be done before Pre-Driver is enabled. This way, as Pre-Driver is enabled and LDO comes out, it will operate in the MP-off mode, as shown in Figure 4-2.

Figure 4-2:VDDG LDO structure



The LDO consists of a power FET MP which delivers current and error amplifier EA which receives reference VREF, compares it to the level of VDDG and drives MP in such a way that voltage at VDDG is equal to voltage of VREF. This control is done via a feedback loop denoted by a blue arrow path.

It is important to note that LDO does not have pull-down capability, it can only pull up VDDG. If LDO is off (Pre-Driver not enabled), the design also guarantees that MP is off. Moreover, even if LDO is on (Pre-Driver is enabled), in case of V(VDDG)>VREF the feedback loop will force error amplifier EA to turn off MP, i.e. no current will be dissipated via MP on chip. Therefore, in reference to Figure 4-2, as VREF is programmed to be below Buck's output voltage of VDDG, it is guaranteed that MP is off and no power will be dissipated in the LDO on chip.

To summarize, in order to use on-board Buck regulator to supply VDDG, the following actions should be taken, in the sequence specified:

1. Enable Buck regulator (using GPIO to enable Buck or having Buck come out after VBAT power up at a cost of additional 310uA in Pre-Driver off condition).
2. Program LDO reference to be smaller than Buck output voltage using LDOGCTL register. The user must make sure the register is writable by enabling proper control register value: write 0xAC to CTLKEY register.
3. Enable Pre-Driver, the LDO will also get enabled but will not supply current to VDDG.

5 Revision history

Table 5-1: Document revision history

Data	Revision	Changes
22-May-2020	1	Initial release.