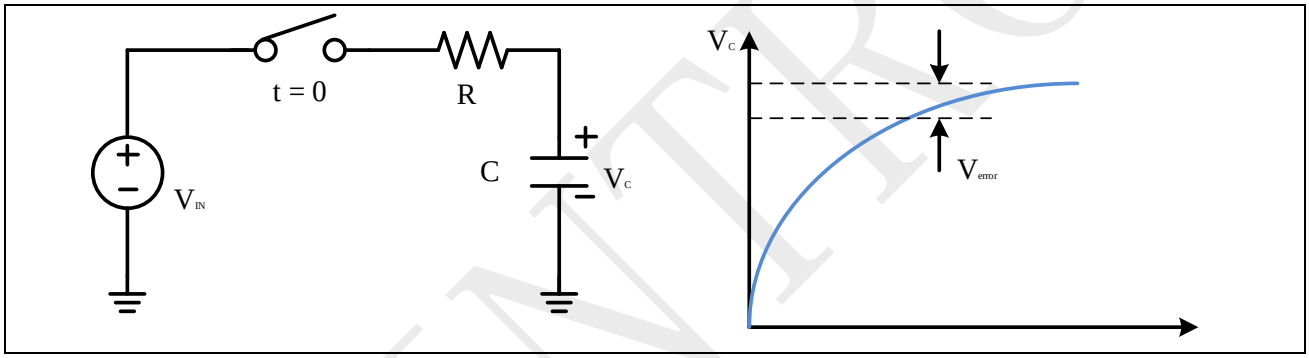
ADC Settling Time Calculation Method

Overview

Capacitive ADCs use a sampling capacitor that is charged to the input signal voltage and utilized by the SAR logic to perform data conversion. Due to the ADC's sampling capacitor, input impedance, and external input circuitry, a settling time is required for the sampling capacitor to reach the input signal voltage. This application note describes a method to calculate the required settling time to achieve accurate ADC measurement results.



This manual applies to:

Applicable Range	
SPC1125 Series	SPC1125，SPC1128
SPC1168 Series	SPC1155，SPC1156，SPC1158，SPC1168，SPD1148，SPD1178，SPD1188，SPD1163，SPM1173
SPC2168 Series	SPC2168，SPC2165，SPC2166，SPC1198
SPC1169 Series	SPC1169，SPD1179，SPD1176，SPD1179B
SPC2188 Series	SPC1185，SPC2188

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Revision History

Version	Date	Author	State	Changes
C/0	2023-04-21	CanChai	Released	1. Initial release.

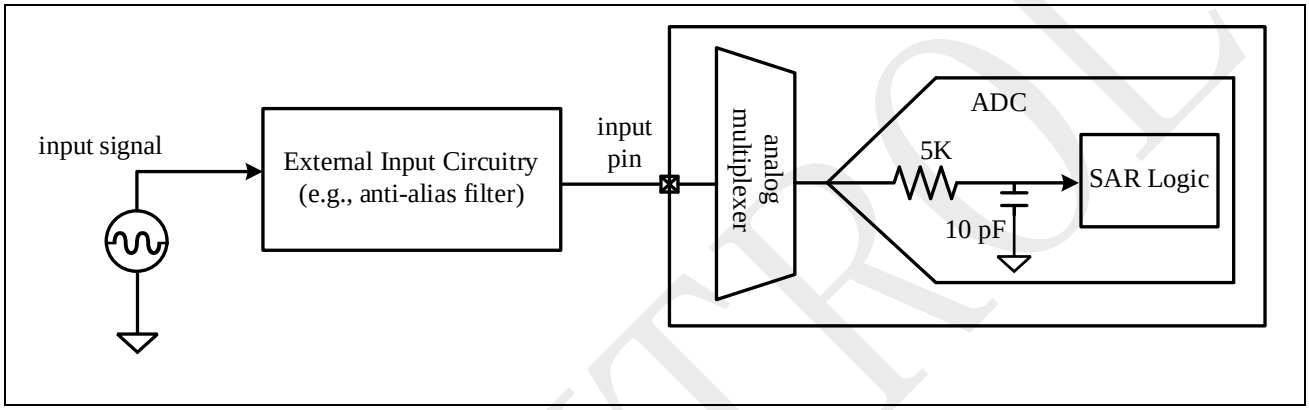
Terms or Abbreviations

Term or Abbreviation	Description
SAR	Successive Approximation Algorithm in ADC models
Settling Time	Time required for the ADC sampling capacitor to charge to the target measurement voltage

1 Equivalent Circuit

To calculate the settling time, this document provides an equivalent circuit that approximates the impedance and capacitance of the ADC circuit (i.e., analog multiplexer, transmission gate, parasitic capacitance, sampling capacitor, etc.). Figure 1-1 shows a lumped-element equivalent circuit that approximates these parameters. The input signal is typically filtered by some external input circuit determined by the system designer, most commonly an anti-aliasing filter connected to the device's input pin, and finally routed to the ADC by the analog multiplexer.

Figure 1-1: Equivalent Circuit for Estimating ADC Settling Time



[1] The resistor and capacitor values in the ADC internal circuit shown in the figure are for demonstration purposes only and do not have actual significance.

2 Factors Affecting Settling Time

For a given application scenario, the required settling time depends on the ADC input circuit, external circuit (e.g., anti-aliasing filter), and the ADC's settling time specifications. If the requirements are not met, the ADC may not achieve the specifications published in the datasheet. Therefore, the settling time of the ADC input circuit, external circuit, and the minimum settling time required by the ADC specifications must be considered to calculate the required settling time.

2.1 Minimum Settling Time

If the ADC input is the output of a PGA in actual use, the settling time is not affected by external circuits as shown in Figure 1-1. In this case, the settling time is the value specified in the ADC design specifications.

If the ADC input is from external devices as shown in Figure 1-1, the impact of external components (e.g., switched capacitors, transmission gates, etc.) on the ADC settling time must be considered. Assuming the settling time specified in the ADC design specifications is 1.5us, in this scenario, the minimum settling time of the ADC can only be referred to as 1.5us because external components also affect the settling time. If the settling time calculated for the external circuit exceeds 1.5us, the ADC settling time will be determined by the external components.

2.2 ADC Input Circuit Settling Time

Since the ADC's equivalent input circuit is an RC circuit, we calculate the settling time in terms of time constants. First, define the settling time as the number of time constants required to achieve the accuracy corresponding to the least significant bit (LSB). The formula for LSB is:

$$LSB = \frac{V_{REF}}{2^N}$$

In the above formula, N is the number of ADC bits.

To calculate the settling time (t) required for the sampling capacitor voltage to reach the input voltage with LSB accuracy, the following equation can be used:

$$V(t) = V_{in} * (1 - e^{\frac{-t}{\tau}})$$

In this formula, V_{in} is the voltage at the device's input pin, and the time constant τ = RC. Expressing t in terms of the number of time constants τ, the result is:

$$t = -\ln\left(1 - \frac{V(t)}{V_{in}}\right) * \tau$$

For example, assuming a full-scale input $V_{in} = V_{REF}$, calculate the voltage value when the input voltage error is 1/4 LSB:

$$V(t) = V_{REF} - \frac{1}{4}LSB = V_{REF} - \frac{1}{4} * \frac{V_{REF}}{2^N} = V_{REF} * (1 - \frac{1}{2^N * 4})$$

Substituting $V(t)$ into the expression for t, we get:

$$t = -\ln\left(1 - \frac{V(t)}{V_{in}}\right) * \tau = -\ln\left(1 - \frac{V_{REF} * (1 - \frac{1}{2^N * 4})}{V_{in}}\right) * \tau = -\ln\left(\frac{1}{2^N * 4}\right) * \tau$$

Assuming the ADC has 12 bits, this formula becomes:

$$t = -\ln\left(\frac{1}{4096 * 4}\right) * \tau = \ln(4096 * 4) * \tau = 9.7 * \tau$$

This formula calculates the settling time for a 12-bit ADC to achieve 1/4 LSB accuracy. If 1/8 LSB accuracy is desired for a 12-bit ADC, the settling time formula becomes:

$$t = -\ln\left(\frac{1}{4096 * 8}\right) * \tau = \ln(4096 * 8) * \tau = 10.4 * \tau$$

As shown in Figure 1-1, assuming R=5Ω and C=10 pF, τ = 50ns can be calculated. Therefore, the settling time required for a 12-bit ADC to achieve 1/4 LSB accuracy is 500ns, and the settling time required for 1/8 LSB accuracy is 520ns.

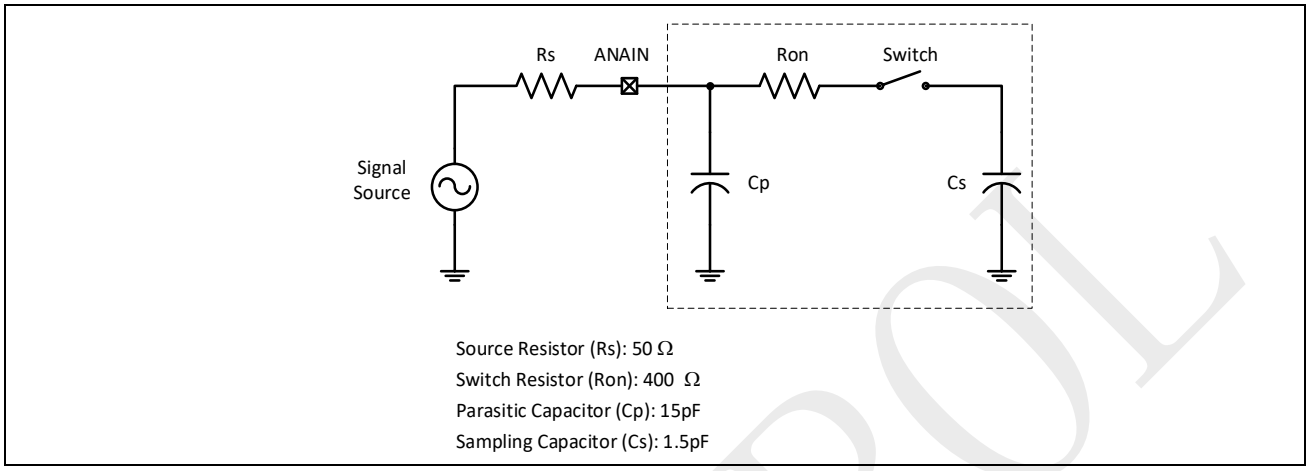
2.3 External Circuit Settling Time

When external circuits are connected to the analog input pin, they affect the ADC settling time. These circuits typically include anti-aliasing filters to remove high-frequency noise that could alias into the signal band of interest. In practical engineering, there are many different filter designs, all of which affect the input impedance and the associated settling time. Therefore, these effects must be considered. If the settling time of the input filter is very long, it will determine the overall system settling time.

3 ADC Settling Time Example Analysis

In practical engineering, the entire ADC-related circuit can be simplified as shown in Figure 3-1.

Figure 3-1: Analog signal diagram



After understanding the calculation method for settling time, we can calculate the required settling time for any system. As shown in the figure above, the factors affecting the settling time of the entire system are: Rs, Ron, Cp, Cs. Since the ADC of the SPC1169 is 13-bit, assuming 1/2 LSB accuracy is required, we can use the previous formula to derive the system settling time as:

$$t = -\ln\left(\frac{1}{2^N * 2}\right) * \tau = \ln(2^{13} * 2) * \tau = \ln(2^{13} * 2) * \big((Rs + Ron) * (Cp + Cs)\big) = 72.01ns$$

Users can calculate the settling time for their specific system based on actual conditions.